

# Compal Confidential

## C1PR2 MB Schematic Document

### LA-E051P

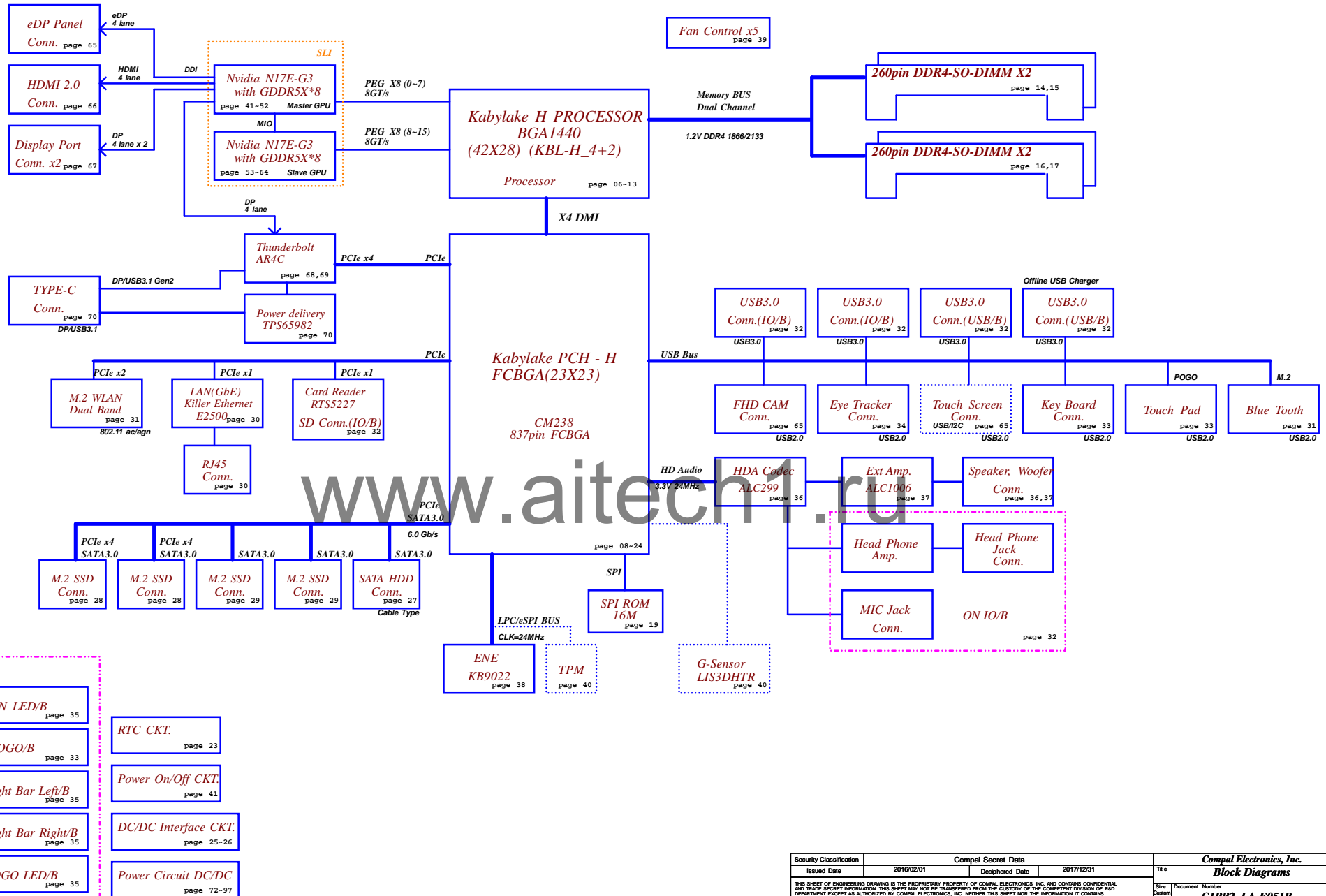
(Eagle 21")

Rev: 1.0

2017-01-09

ZZZ DA@  
PCB 1SJ LA-E051P REV1 MB  
DAC00006010

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				Size	Document Number
				Custom	C1PR2 LA-E051P
				Date:	Monday, January 09, 2017
				Sheet	1 of 103
				Rev	1.0



Compal Secret Data				Compal Electronics, Inc.		
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				Date:	Monday, January 09, 2017	Sheet 2 of 103

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	V <sub>BI</sub> D min	V <sub>BI</sub> D typ	V <sub>BI</sub> D max	EC AD
0	0		0.000 V	0.300 V	0x00 - 0x13
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 - 0x1E
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64
8	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76
9	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77 - 0x87
10	130K +/- 1%	1.849 V	1.865 V	1.881 V	0x88 - 0x96
11	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97 - 0xA4
12	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA5 - 0xAF
13	240K +/- 1%	2.316 V	2.329 V	2.343 V	0xB0 - 0xB7
14	270K +/- 1%	2.395 V	2.408 V	2.421 V	0xB8 - 0xBF
15	330K +/- 1%	2.521 V	2.533 V	2.544 V	0xC0 - 0xC9
16	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA - 0xD4
17	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD5 - 0xDD
18	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDE - 0xFD
19	NC	3.000 V	3.000 V		0xFF1 - 0xFF

BUS	Device	Address(7 bit)	Address(8bit)	
			Write	Read
I2C_0 (+3VS)	N/C			
I2C_1 (+3VALW)	N/C			
PCH_SMBCLK (+3VS)	DIMM1			
	DIMM2			
	DIMM3			
	DIMM4			
	LIS3DHTR(G-sensor)	0x30		
EC_SMB_CK1 (+3VLP)	BQ24780 (Charger IC)	0x12		
	BATTERY PACK	0x16		
EC_SMB_CK3 (+3VALW)	PD(TPS65982)	0x00		
	59116 (LED driver, M/B)	0xC0		
	59116 (LED driver, USB/B)	0xC2		
EC_SMB_CK2 (+3VS)	N17E-G3 (Master)	0x9E		
	N17E-G3 (Slave)	0x9C		
	AMP for SPK(ALC1006)	0x24		
	AMP for Woofer(ALC1006)	0x26		
	HP AMP (SV3S700)	0xE4		
	External Thermal Sensor	0x4D		

[illegible]

<i>STATE</i> \ <i>SIGNAL</i>	<i>SLP_S3#</i>	<i>SLP_S4#</i>	<i>SLP_S5#</i>	<i>+VALW</i>	<i>+V</i>	<i>+VS</i>	<i>Clock</i>
<i>S0 (Full ON)</i>	<i>HIGH</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>
<i>S3 (Suspend to RAM)</i>	<i>LOW</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>
<i>S4 (Suspend to Disk)</i>	<i>LOW</i>	<i>LOW</i>	<i>HIGH</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>
<i>S5 (Soft OFF)</i>	<i>LOW</i>	<i>LOW</i>	<i>LOW</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>

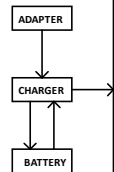
[illegible]

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

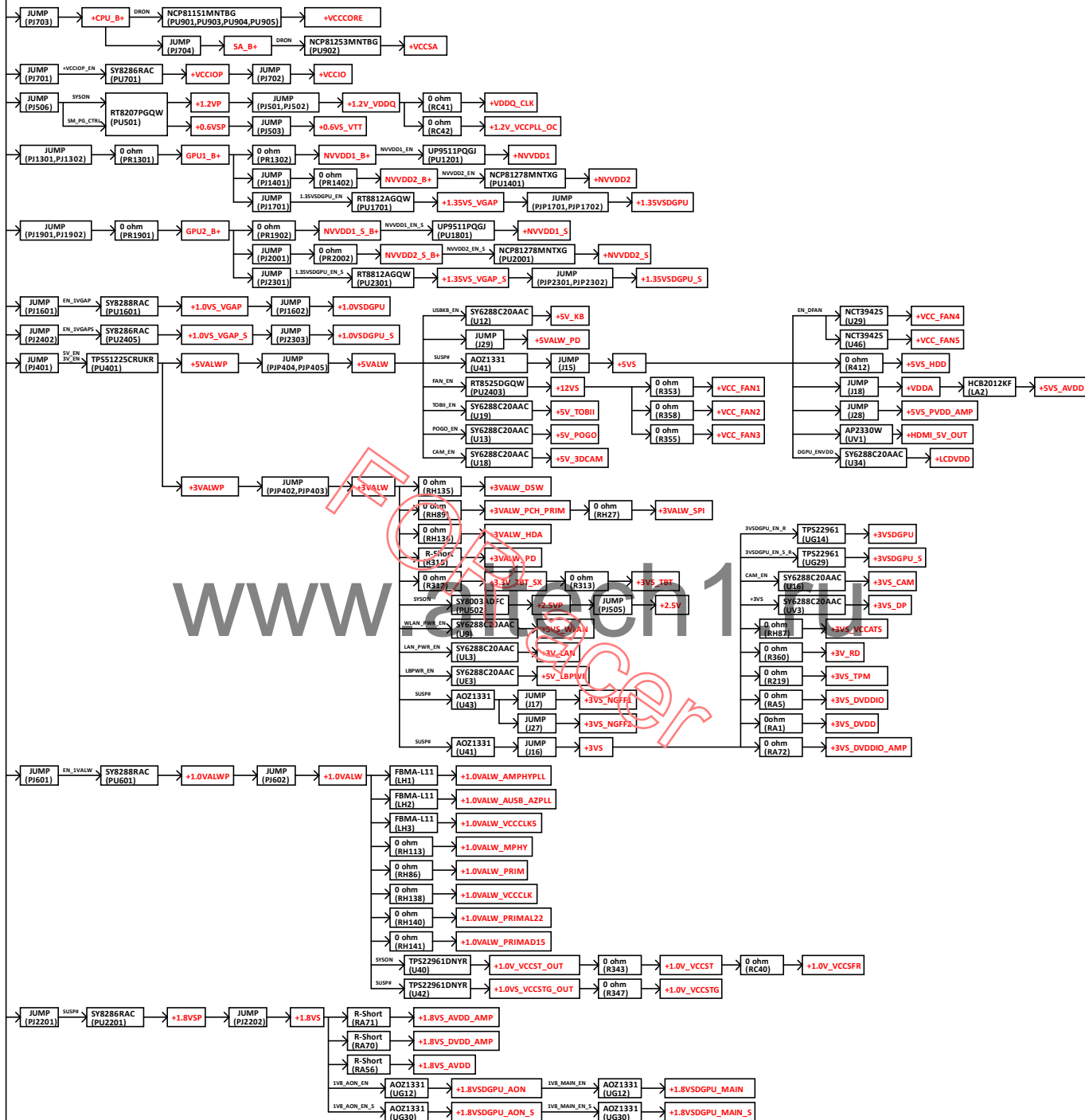
Power Plane	Description	S0	S3	S4	S5
+RTCVCC	RTC Battery Power	ON	ON	ON	ON
+19V_VIN	Adapter power supply	N/A	N/A	N/A	N/A
+17.4V_BATT	Battery power supply	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A	N/A
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+5VALW	+5V Always power rail	ON	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON
+3VALW_PCH_PRIM	+3VALW power for PCH power rails	ON	ON	ON	ON*
+3VALW_SPI	+3VALW_PRIM supply for the SPI IO	ON	ON	ON	ON
+1.0VALW	+1.0V Always power rail	ON	ON	ON	ON
+1.2V_VDDQ	DDR IV +1.2V power rail	ON	ON	OFF	OFF
+1.0V_VCCST	Sustain voltage for processor in Standby modes	ON	ON	OFF	OFF
+5VS	System +5V power rail	ON	OFF	OFF	OFF
+3VS	System +3V power rail	ON	OFF	OFF	OFF
+1.0VS_VCCSTG	+1.0VALW_PRIM Gated version of VCCST	ON	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.675VS power rail for DDR terminator .	ON	OFF	OFF	OFF
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF	OFF
+VCCIO	CPU IO power rail	ON	OFF	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF	OFF
+3VSDGPU	+3VS power rail for GPU circuit	ON	OFF	OFF	OFF
+1.8VSDGPU_AON	+1.8VALW power rail for GPU(AON rails)	ON	OFF	OFF	OFF
+1.8VSDGPU_MAIN	+1.8VS power rail for GPU GC6	ON	OFF	OFF	OFF
+NVVDD1	Core voltage for VGA	ON	OFF	OFF	OFF
+NVVDD2	Core voltage for VGA	ON	OFF	OFF	OFF
+1.35VSDGPU	+1.5VS power rail for GPU	ON	OFF	OFF	OFF
+1.0VSDGPU	+1.05VS power rail for GPU	ON	OFF	OFF	OFF

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

NV_name	COMPAL_name
NVVD	+NVVD1
NVVD5	+NVVD2
FDVD	+1.35VSDGPU
FBVDQ	+1.35VSDGPU
VPP	+1.8VSDGPU_AON
IFP_IOVD	+1.0VSDGPU
IFPx_PLLVD	+1.8VSDGPU_MAIN
PEX_DVD	+1.0VSDGPU
PEX_HVD/PEX_PLL_HVD	+1.8VSDGPU_MAIN
FBx_PLL_AVDD	+1.8VSDGPU_MAIN
GPCPLL_AVDDx/Core_PLLVD	+1.8VSDGPU_MAIN
VID_PLLVD	+1.8VSDGPU_MAIN
SP_PLLVD	+1.8VSDGPU_MAIN
V18_MAIN	+1.8VSDGPU_MAIN
V18_AON	+1.8VSDGPU_AON



B+





BIOS : 0.04

AC mode

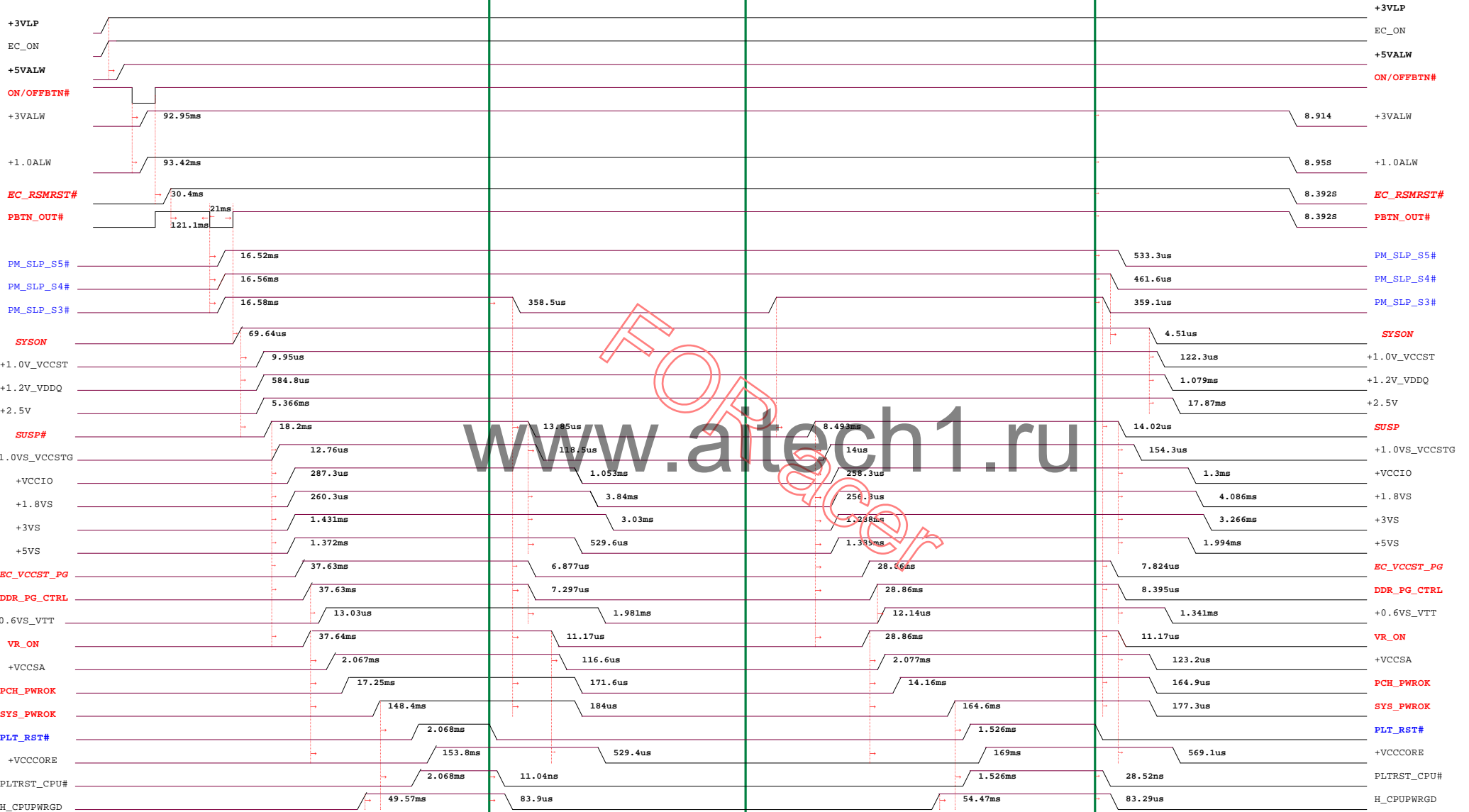
Power On

S3

S3 Resume

Power Off

Plug in

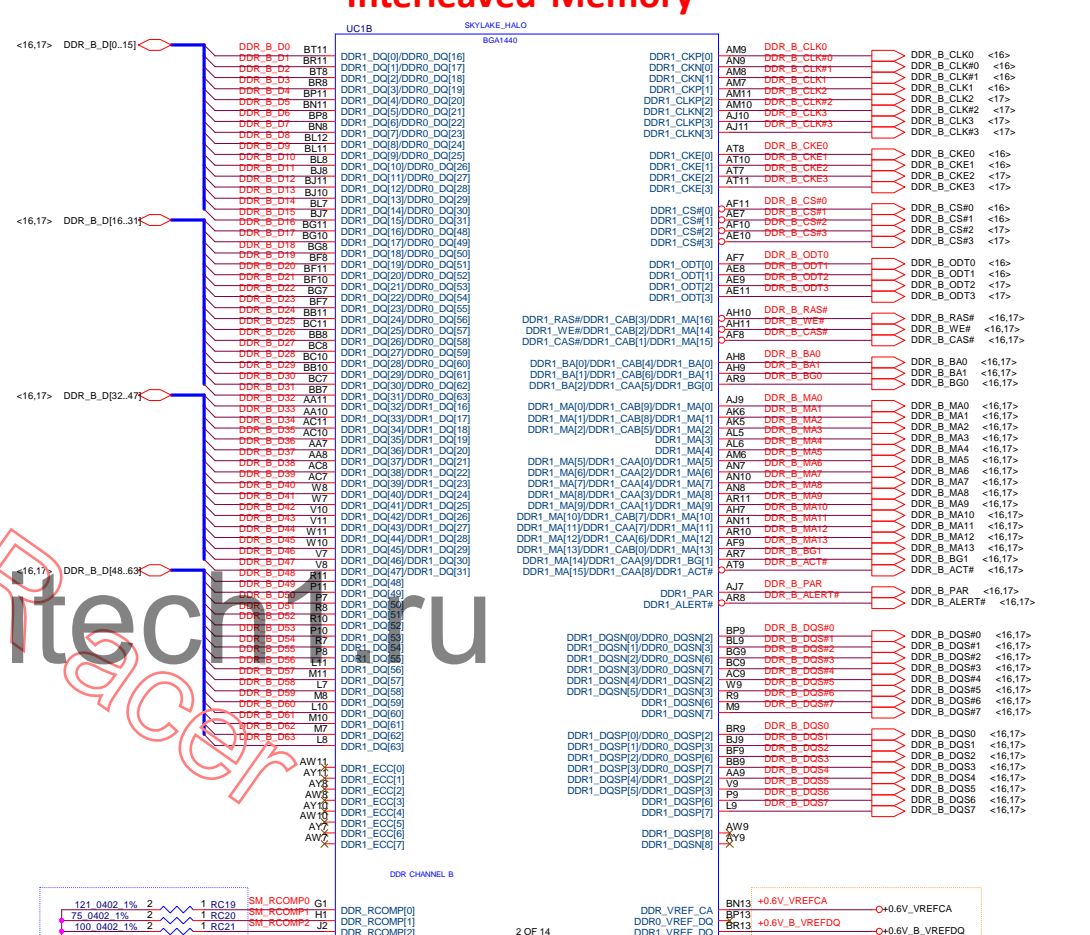


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				Custom	C1PR2 LA-E051P	1.0
				Date:	Monday, January 09, 2017	Sheet 5 of 103



## CHANNEL-B

### Interleaved Memory

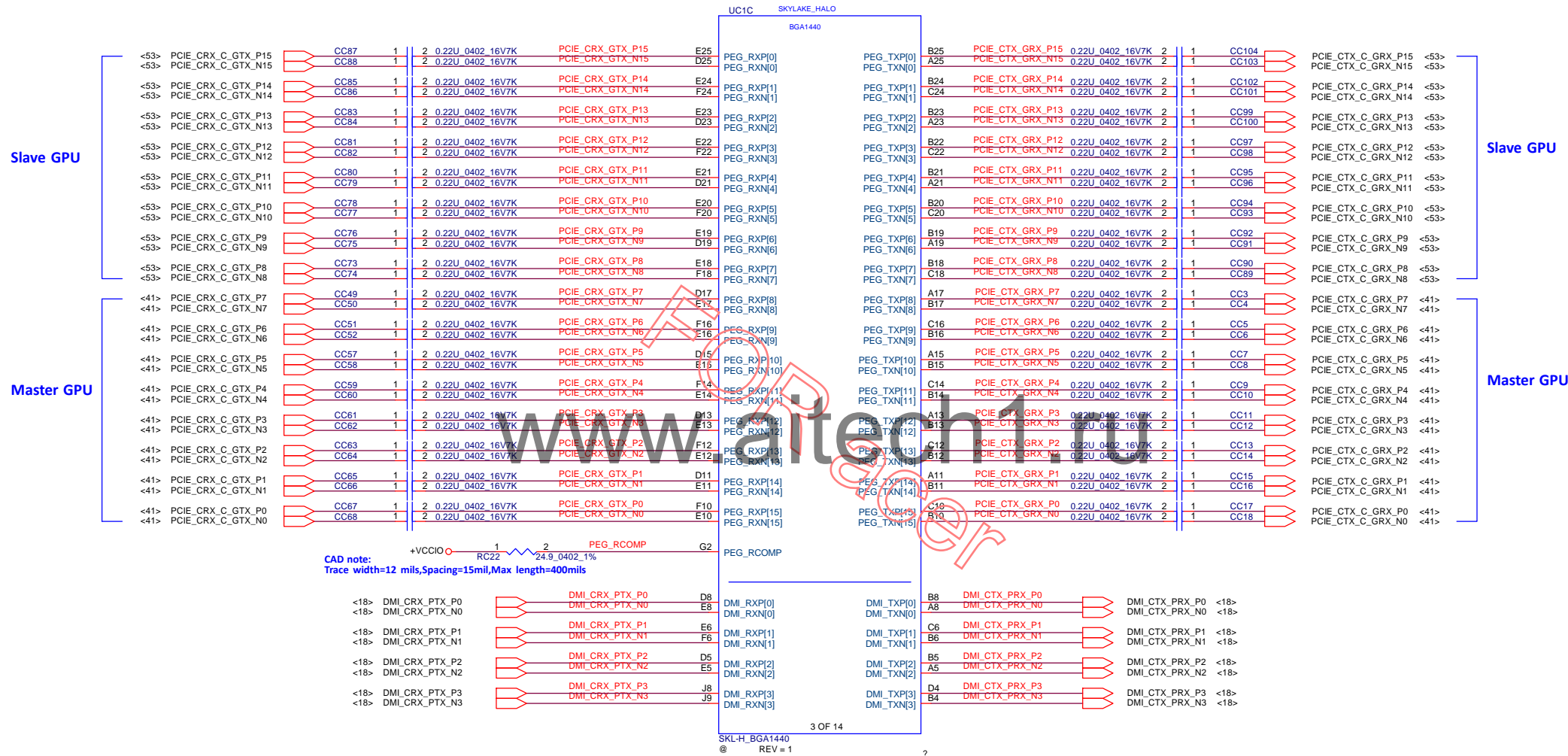


Timing diagram for SM\_RCOMP0, SM\_RCOMP1, and SM\_RCOMP2 signals. The diagram shows three signals (RC19, RC20, RC21) with a period of 100.0402 ns and a duty cycle of 2%. The signals are connected to DDR\_RCOMP0, DDR\_RCOMP1, and DDR\_RCOMP2. The DDR\_RCOMP signals are connected to DDR\_VREF\_CA, DDR\_VREF\_DO, and DDR\_VREF\_DQ. The DDR\_VREF signals are connected to +0.6V\_VREFCA, +0.6V\_B\_VREFDQ, and +0.6V\_VREFDQ. The diagram is labeled "Place close to CPU" and "2 OF 14".

SM\_RCOMP0  
SM\_RCOMP1  
SM\_RCOMP2  
Trace = 12-15 mils  
Spacing = 20 mils  
Max length = 500 mils

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				Custom	<b>C1PR2 LA-E051P</b>	1.0
				Date:	Monday, January 09, 2017	Sheet 7 of 103

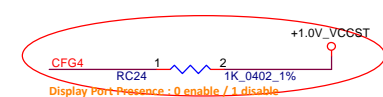
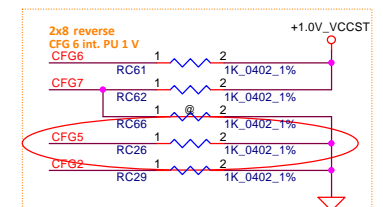
# PEG 2x8 reverse



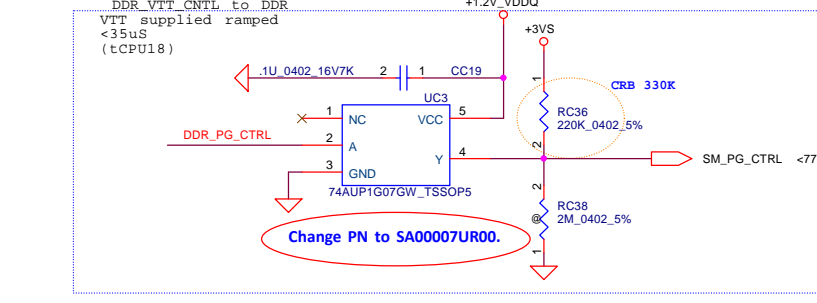
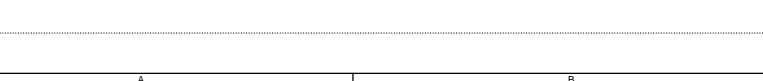
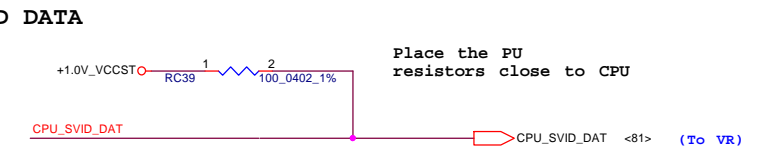
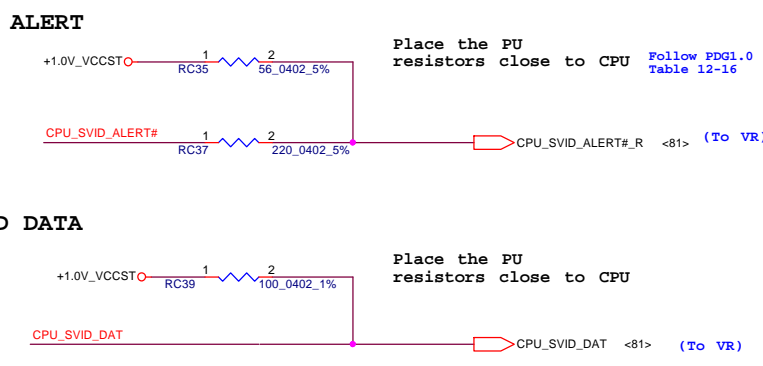
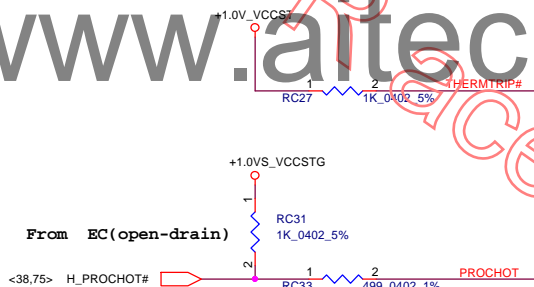
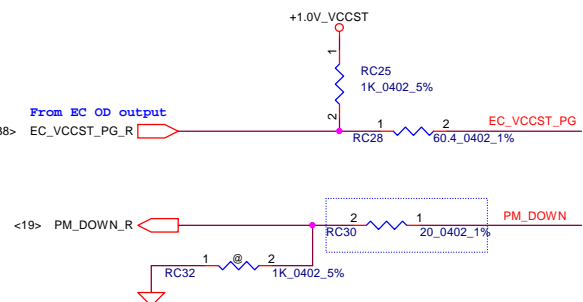
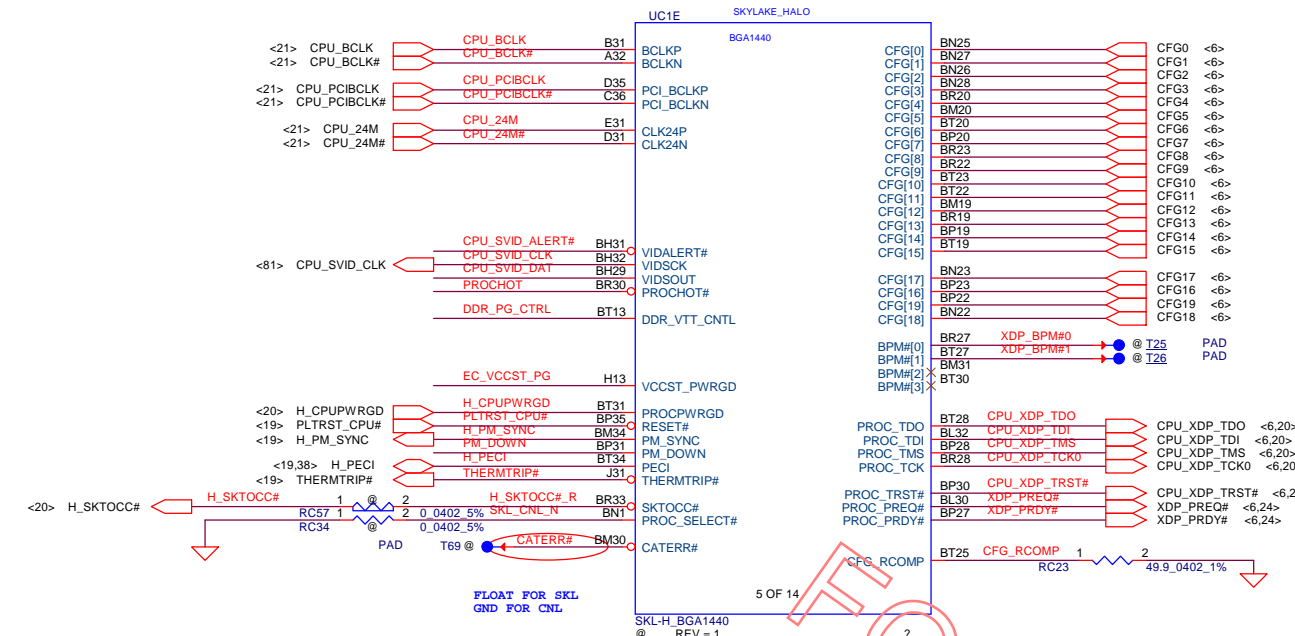
Reference SKL EDS 0.85 Table 6-8  
CFG signals internal PH default value = 1

	Description
CFG[0] *	Stall reset sequence after PCU PLL lock until de-asserted - 1 = (Default) Normal Operation; No stall. - 0 = Stall.
CFG[4] *	Enable eDP - 1 = Disabled. - 0 = Enabled.
CFG[7] *	PEG Training: - 1 = (default) PEG Train immediately following RESET# de assertion. - 0 = PEG Wait for BIOS for training
CFG[1] CFG[3] CFG[8:19]	Reserved configuration lane.

PCIE pore assign	Config. Signals		
	CFG[6]	CFG[5]	CFG[2]
1 x 16	1	1	1
1 x 16 reverse	1	1	0
2 x 8	1	0	1
2 x 8 reverse *	1	0	0
1 x 8	0	0	1
1x8+2x4 reverse	0	0	0



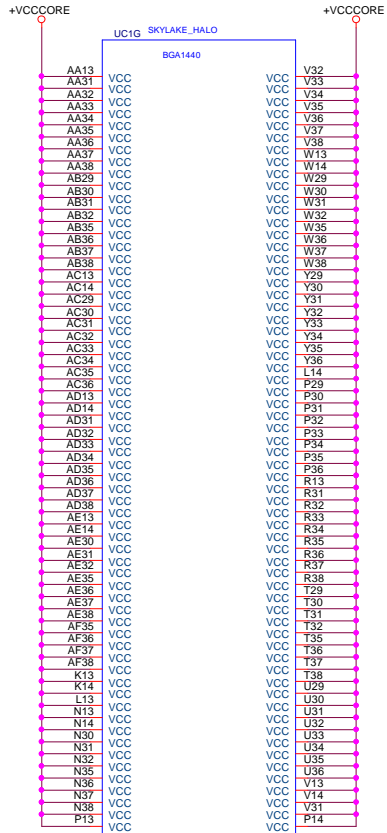
www.aitech1.ru



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				Custom	C1PR2 LA-E051P
				Date	Monday, January 09, 2017
				Sheet	9 of 103



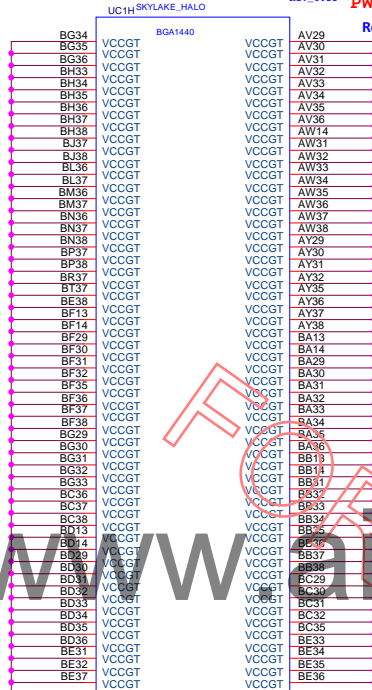
VCC 27A (U 15W Dual Core Q72)



Trace Length < 25 mils

VCC\_SENSE <B1>  
VSS\_SENSE <B1>

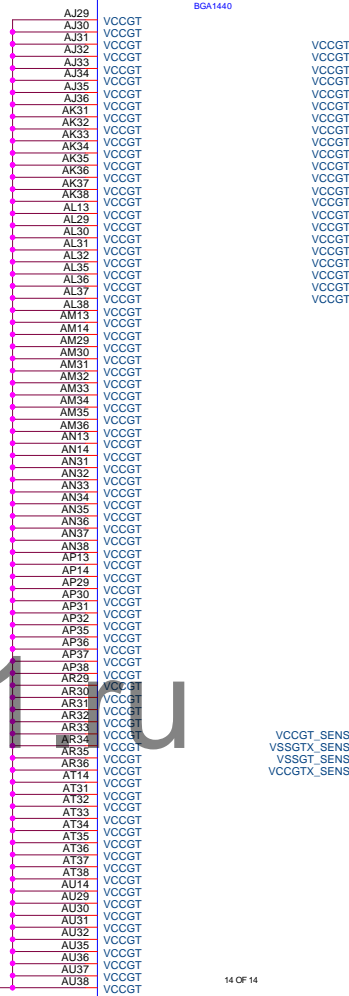
Rev\_0.53 PWR remove VCCGT 3/10  
Reserve resistor to Gnd



SKL-H\_BGA1440  
REV = 1

RC67  
0\_0402\_5%

UC1N SKYLAKE\_HALO



DEL VCCGT net 3/16

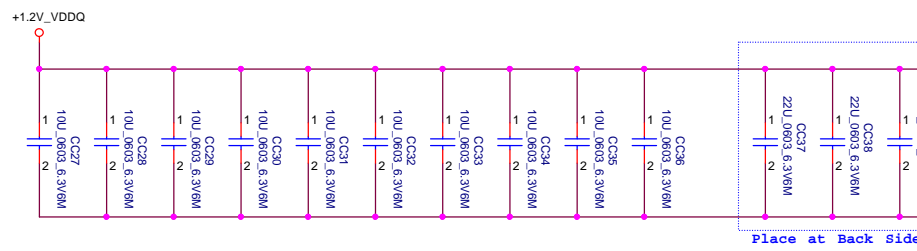
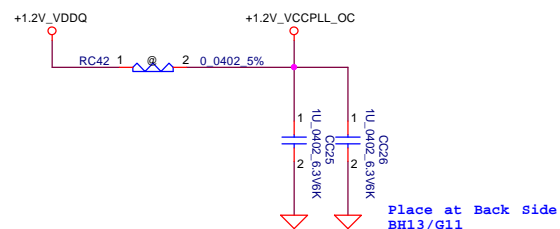
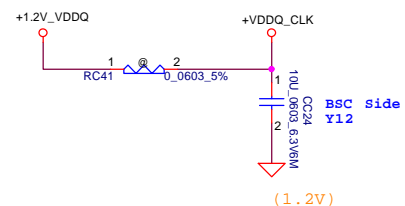
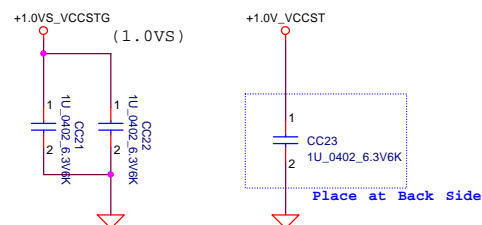
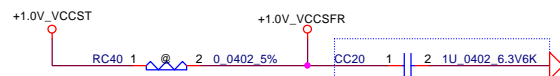
EDS:Rail is unconnected for Processors without GT3/4.

VCCGT\_SENSE  
VSSGT\_SENSE  
VSSGT\_SENSE  
VCCGTX\_SENSE

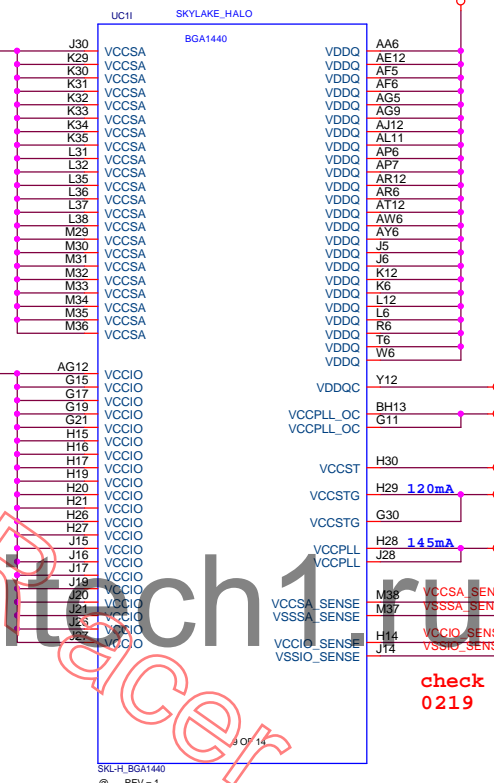
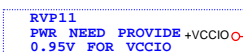
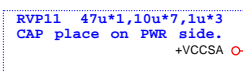
Trace Length < 25 mils

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Date:		Monday, January 09, 2017		Sheet		10 of 103					

CPU\_CORE/VCCGT/VCCSA decoupling capacitor place to PWR side

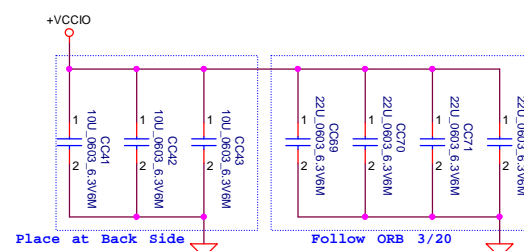


```
+1.35V_VDDQ_CPU : 10UF/6.3V/0603 *10
                  22UF/6.3V/0603 * 4
update CRB cap QTY
```

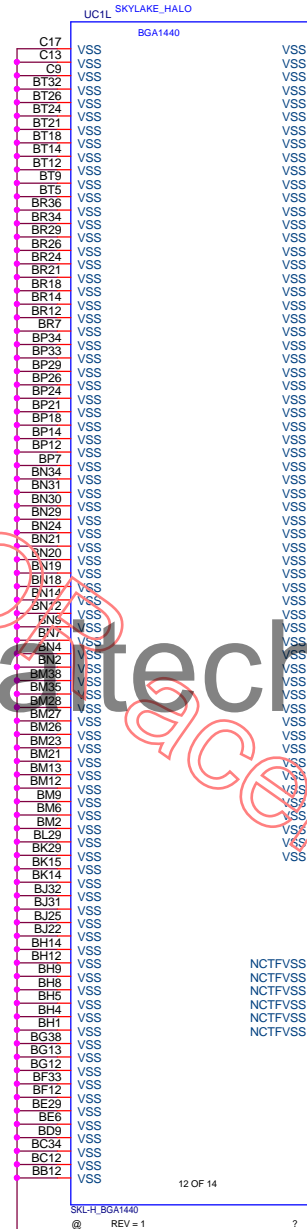
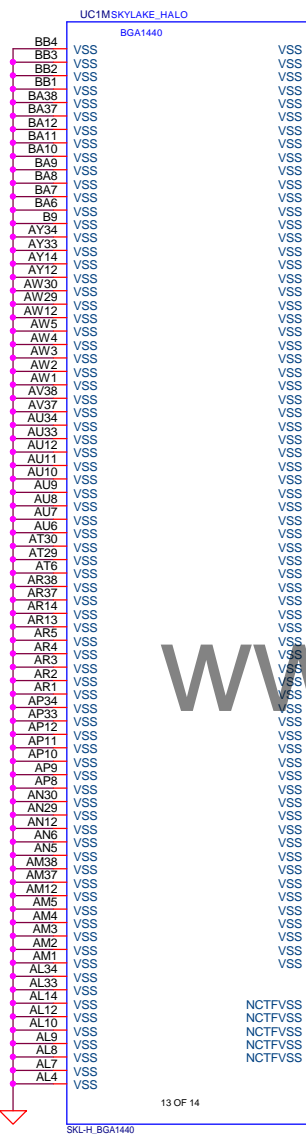
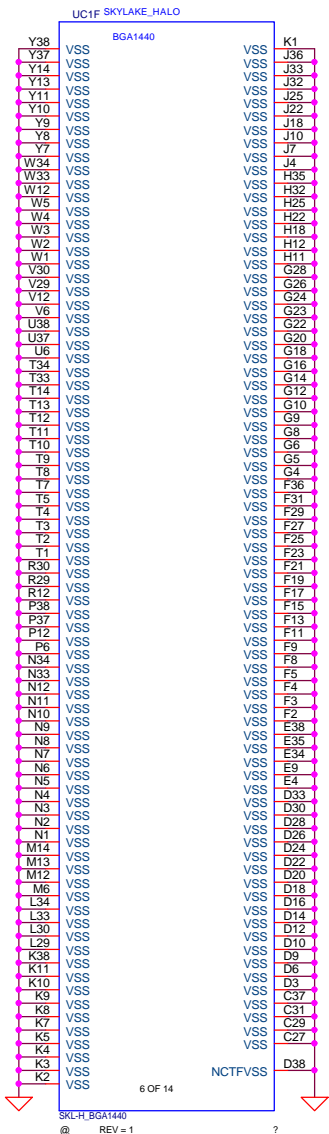


check PH/PL on pwr side ??  
0219 NOTE:

**NOTE:**  
VCCPLL\_OC is allowed to be turned off during S3 & DS3 if it is not powered directly from VDDQ

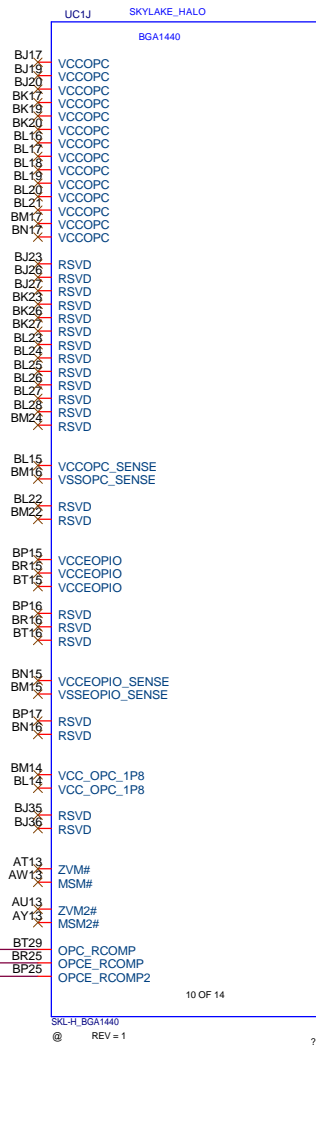


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				Size	Document Number
				Date	Rev
				C1PR2 LA-E051P	1.0
Date: Monday, January 09, 2017				Sheet 11 of 103	



EDRAM

CRB EDRAM





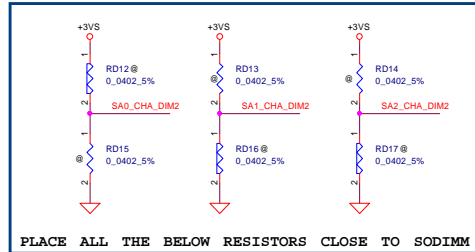


conn need link

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				<b>C1PR2 LA-E051P</b>		
Date:				Monday, January 09, 2017	Sheet	14 of 103

# CHANNEL-A BOT DIMM2

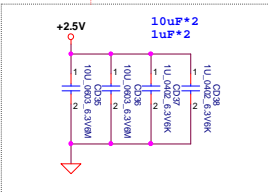
BOT: JDIMM2 CONN Non-ECC DIMM



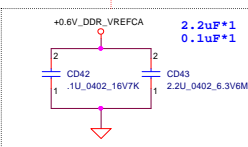
SPD ADDRESS FOR CHANNEL A :  
WRITE ADDRESS: 0XA2  
READ ADDRESS: 0XA3  
SA0 = 1; SA1 = 0; SA2 = 0.  
DDR4 POR OPERATING SPEED: 1867 MT/S  
STRETCH GOAL IS 2133 MT/S

Layout Note:  
Place near JDIMM2.257,259

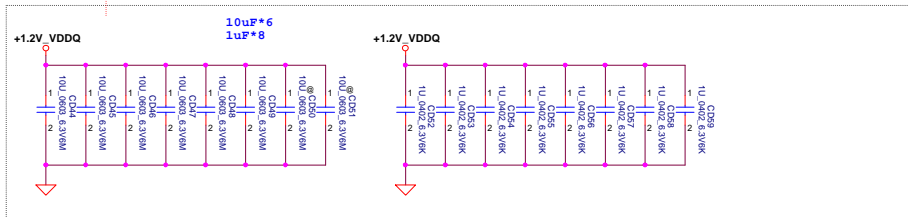
Layout Note:  
Place near JDIMM2.258



Layout Note:  
PLACE THE CAP WITHIN 200 MILS FROM THE JDIMM2

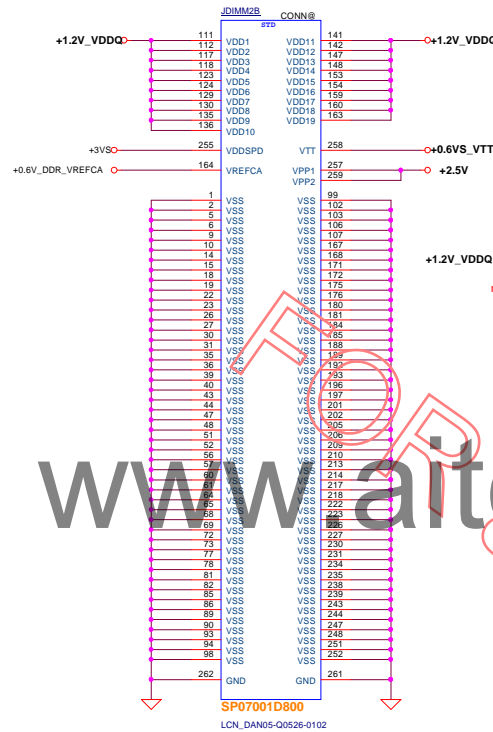


Layout Note:  
Place near JDIMM2

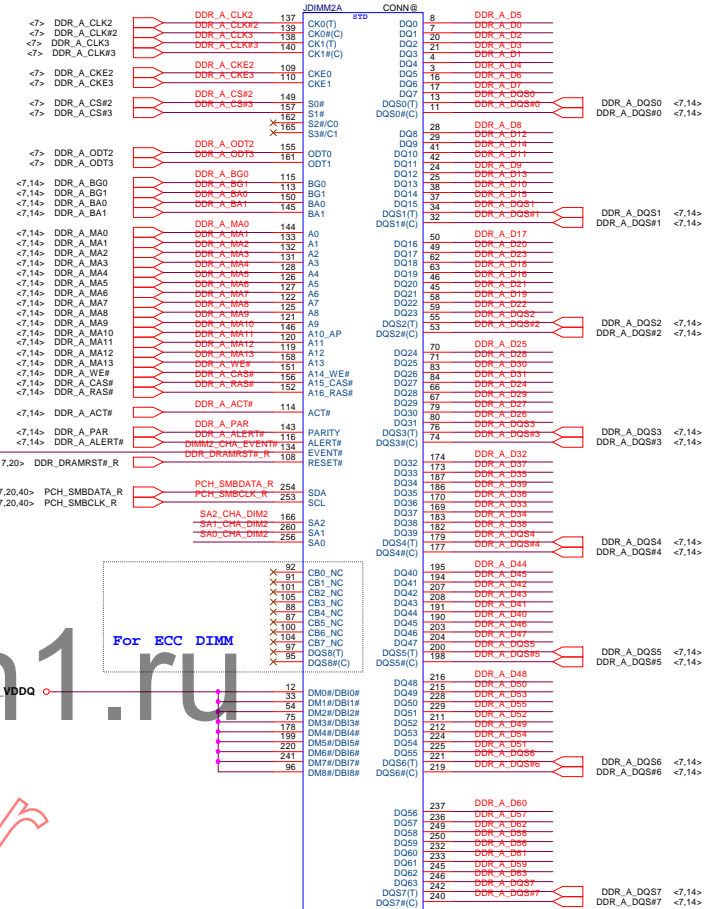


## Interleaved Memory

<7,14> DDR\_A\_D[0..15]  
<7,14> DDR\_A\_D[16..31]  
<7,14> DDR\_A\_D[32..47]  
<7,14> DDR\_A\_D[48..63]

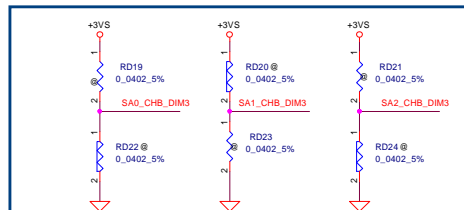


STD (5.2 mm) conn need link



## TOP DIMM3

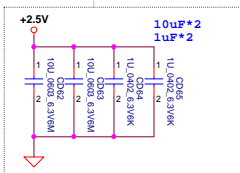
TOP: JDIMM3 CONN Non-ECC DIMM



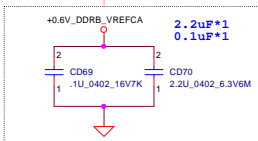
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

```
SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S
```

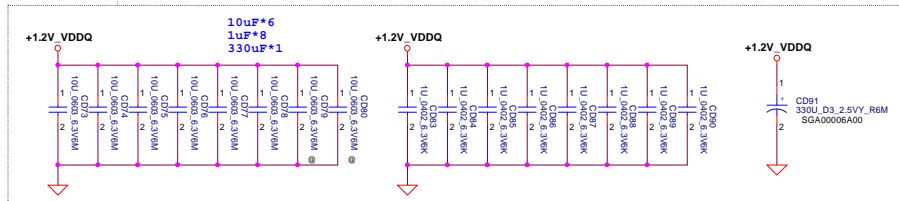
Layout Note:  
Place near JDIMM3.257,259



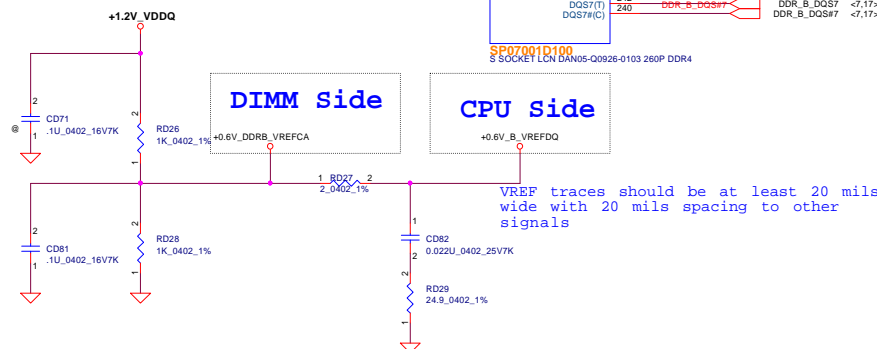
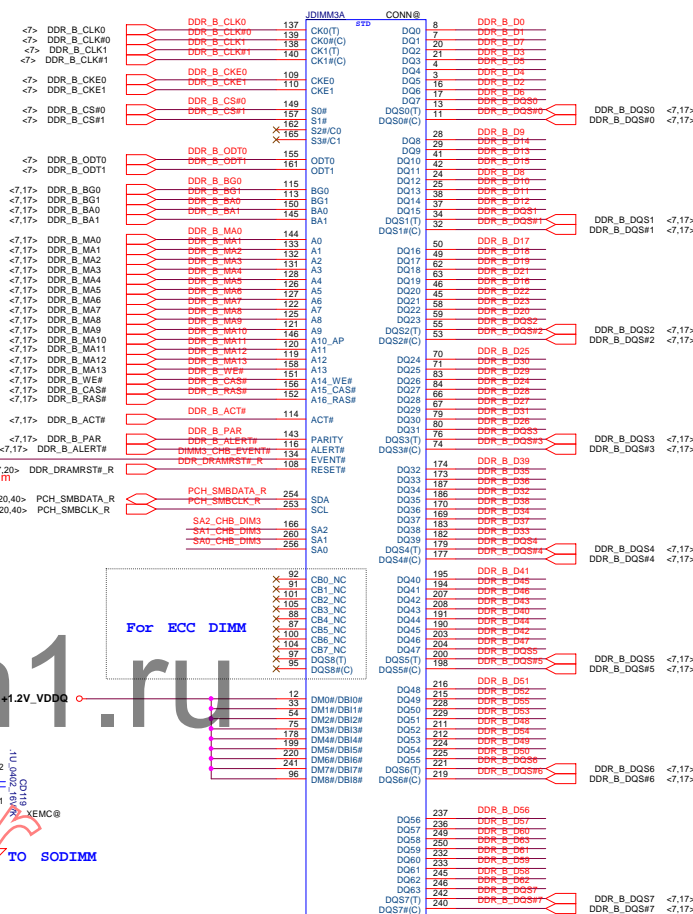
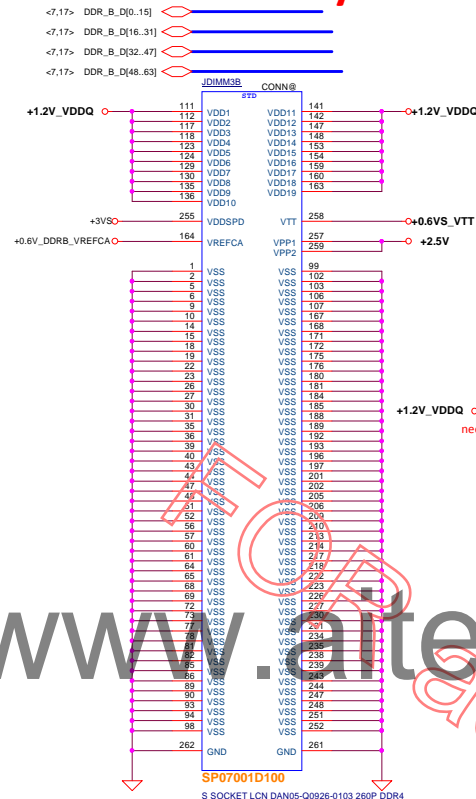
Layout Note:  
PLACE THE CAP WITHIN 200 MILS  
FROM THE JDIMM3



Layout Note:  
Place near JDIMM3



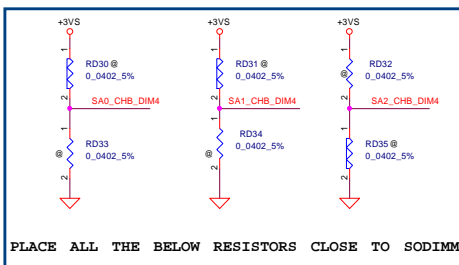
REVERSE TYPE (9.2 mm) conn need link



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				CIPR2 LA-E05P1 Date: Monday, January 09, 2017	
				Sheet	16 of 103

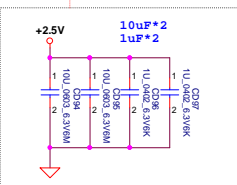
**BOT DIMM4**

BOT: JDIMM4 CONN Non-ECC DIMM

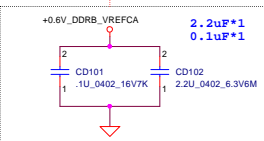


```
SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA6
READ ADDRESS: 0XA7
SA0 = 1; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S
```

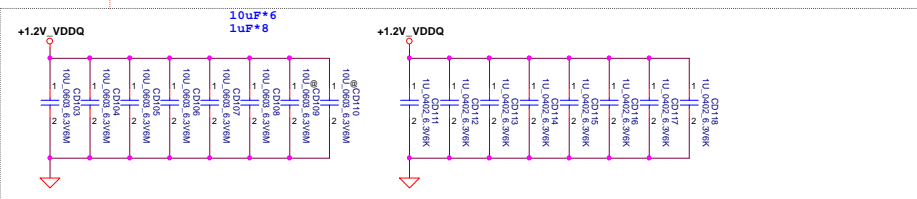
Layout Note:  
Place near JDIMM4.257,259



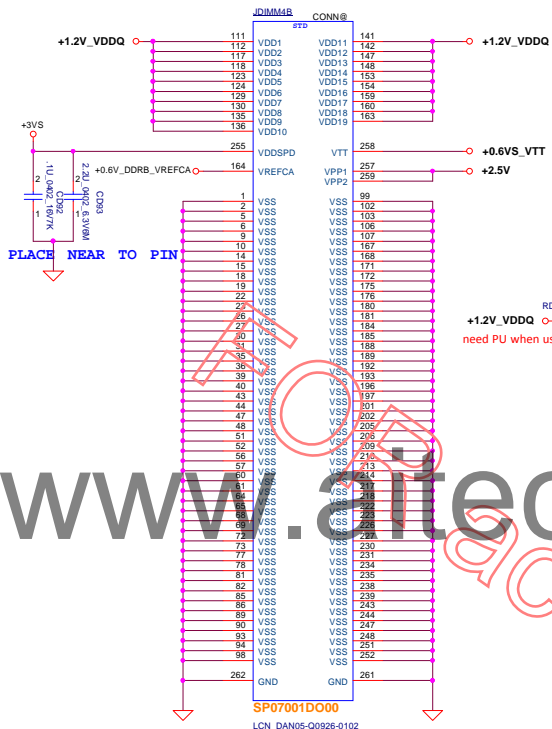
Layout Note:  
PLACE THE CAP WITHIN 200 MILS  
FROM THE JDIMM4



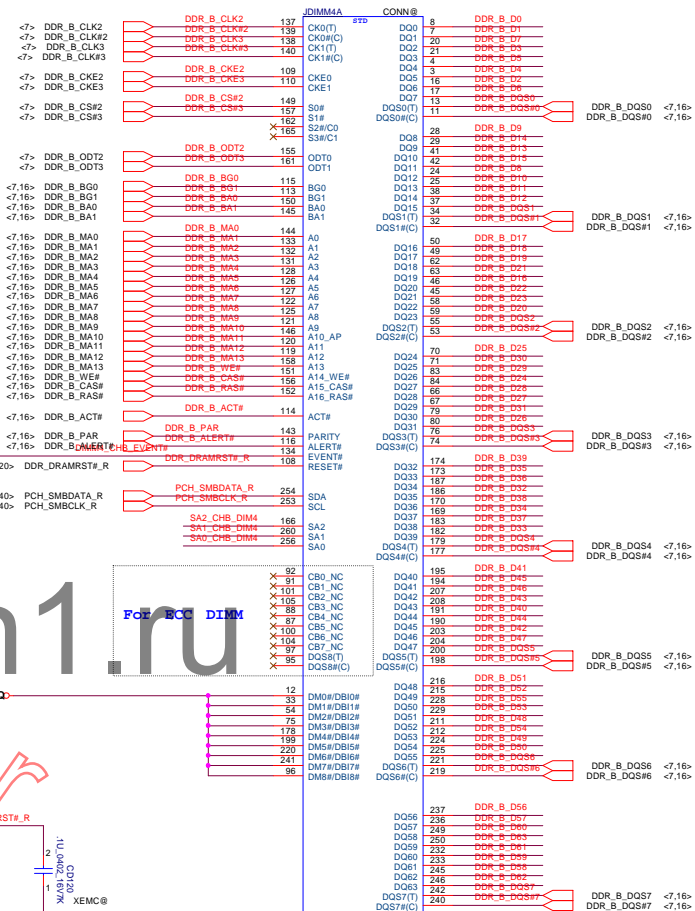
Layout Note:  
Place near JDIMM4



## Interleaved Memory



STD (9.2 mm) conn need link

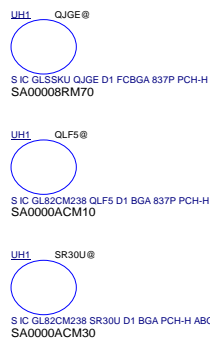


PLACE NEAR  TO SODIMM

SP07001DO00  
LCN\_DAN05-Q0926-0102

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				C1PR2 LA-E051P	
				Date:	Monday, January 09, 2017
				Sheet	17 of 103





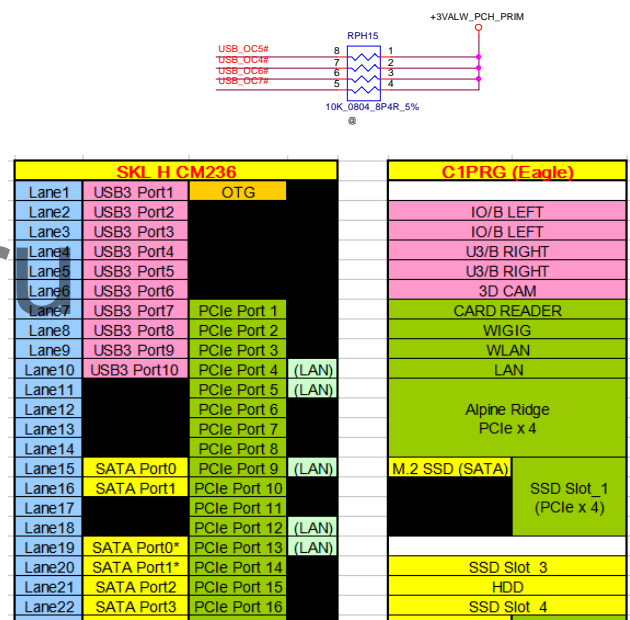
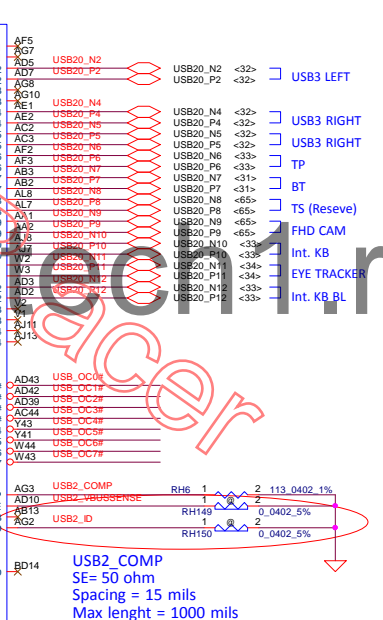
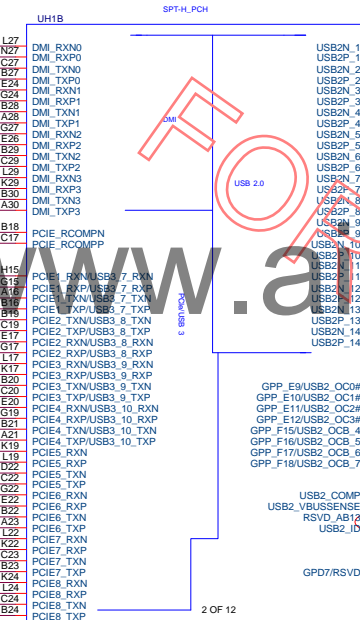
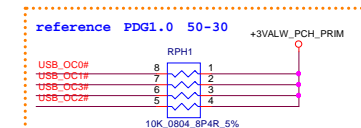
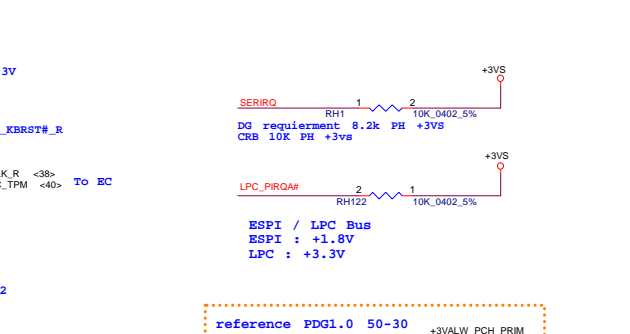
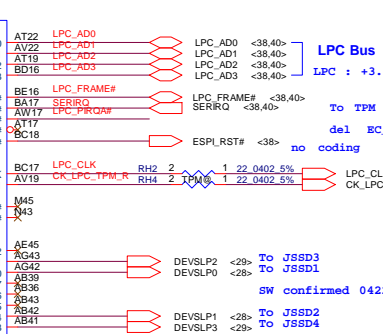
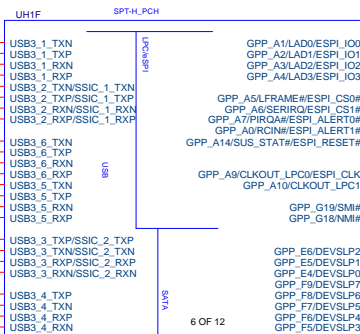
10 Board (left side)  
back

3D CAM

U3 Board (right side)  
front

U3 Board (right side)  
back

CHECK ACER DVR for port use  
front panel spec 5"  
int cable 15"



#546884 P.231 PCIE\_RCOMP/PCIE\_RCOMP  
BO=4 W=12~15 S=12 R=100ohm

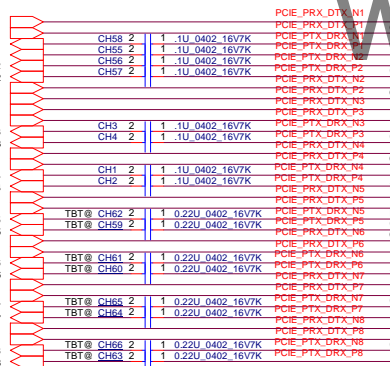
CARD READER

WIGIG

WLAN

LAN

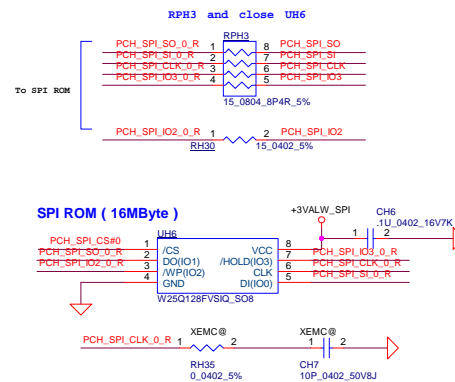
Thunderbolt



SKL-H-PCH\_BGA837  
REV = 1.3

SKL-H CM236			C1PRG (Eagle)		
Lane1	USB3 Port1	OTG			IO/B LEFT
Lane2	USB3 Port2				IO/B LEFT
Lane3	USB3 Port3				U3/B RIGHT
Lane4	USB3 Port4				U3/B RIGHT
Lane5	USB3 Port5				3D CAM
Lane6	USB3 Port6				CARD READER
Lane7	USB3 Port7	PCle Port 1			WIGIG
Lane8	USB3 Port8	PCle Port 2			WLAN
Lane9	USB3 Port9	PCle Port 3			LAN
Lane10	USB3 Port10	PCle Port 4 (LAN)			Alpine Ridge PCle x4
Lane11		PCle Port 5 (LAN)			
Lane12		PCle Port 6			
Lane13		PCle Port 7			
Lane14		PCle Port 8			
Lane15	SATA Port0	PCle Port 9 (LAN)			
Lane16	SATA Port1	PCle Port 10			M.2 SSD (SATA)
Lane17		PCle Port 11			SSD Slot_1 (PCle x4)
Lane18		PCle Port 12 (LAN)			
Lane19	SATA Port0*	PCle Port 13 (LAN)			
Lane20	SATA Port1*	PCle Port 14			SSD Slot_3
Lane21	SATA Port2	PCle Port 15			HDD
Lane22	SATA Port3	PCle Port 16			SSD Slot_4
Lane23	SATA Port4	PCle Port 17			
Lane24	SATA Port5	PCle Port 18			M.2 SSD (SATA)
Lane25		PCle Port 19			SSD Slot_2 (PCle x4)
Lane26		PCle Port 20			
USB20	USB2 Port1				IO/B LEFT
USB20	USB2 Port2				IO/B LEFT
USB20	USB2 Port3				U3/B RIGHT
USB20	USB2 Port4				U3/B RIGHT
USB20	USB2 Port5				TP Slide module
USB20	USB2 Port6				BT (NGFF)
USB20	USB2 Port7				Touch Screen
USB20	USB2 Port8				FHD CAM
USB20	USB2 Port9				Int. KB
USB20	USB2 Port10				TOBII EYE TRACKER
USB20	USB2 Port11				

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13
CM236 / C236	USB 3.0/ OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0/ PCIe	USB 3.0/ PCIe	USB 3.0/ PCIe	USB 3.0/ PCIe/ LAN	PCIe/ LAN	PCIe	PCIe
SKU	14	15	16	17	18	19	20	21	22	23	24	25	26
CM236 / C236	PCIe	SATA0 <sup>1</sup> / PCIe/ LAN	SATA1 <sup>1</sup> / PCIe	PCIe	PCIe/ LAN	SATA0 <sup>1</sup> / PCIe/ LAN	SATA1 <sup>1</sup> / PCIe	SATA/ PCIe	SATA/ PCIe	SATA/ PCIe	SATA/ PCIe	SATA/ PCIe	SATA/ PCIe



**SPIO\_MOSI**  
int. PH  
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direct i on dui ng strap sampling.

---

**SPIO\_MISO**  
int. PH  
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direct i on dui ng strap sampling.

---

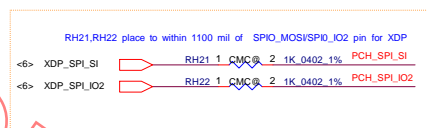
**SPIO\_I02**  
int. PH  
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direct i on dui ng strap sampling.

---

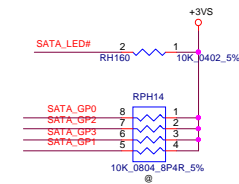
**SPIO\_I03**  
int. PH  
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direct i on dui ng strap sampling.

---

**GPIO\_I12**  
int. PD  
This strap should sample LOW.



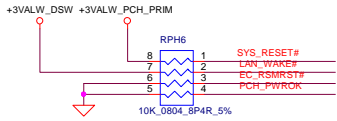
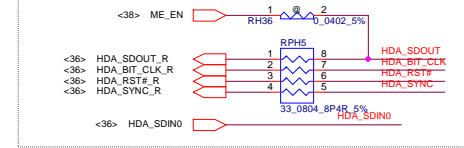
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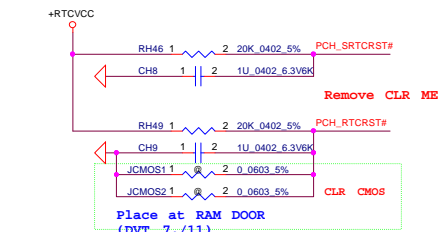
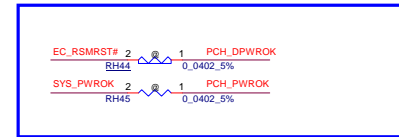
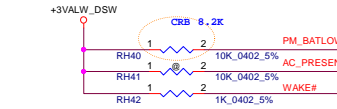
	GPP_F13 DGPU_PRSNT#
DIS	0
<del>UMA</del>	<del>1</del>

Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b> <b>PCH(2/7)SPI,SATA,XDP</b>		
Issued Date	2016/02/01	Deciphered Date	2017/12/31	Title		
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				Custom	C1PR2 LA-E051P	1.0
				Date:	Monday, January 09, 2017	Sheet 19 of 103

## HDA for AUDIO



Follow 543016\_SKL\_U\_V\_PDG\_0\_9



## Functional Strap Definitions

**SMBALERT# / GPP\_C2**  
int. PD  
0 = Disable Intel ME (TLS) (Default)  
1 = Enable Intel ME (TLS)

**SML0ALERT# / GPP\_C5**  
int. PD  
0 = LPC Is selected for EC. (Default)  
1 = eSPI Is selected for EC.

**SML1ALERT# / PCHHOT# / GPP\_B23**  
int. PD

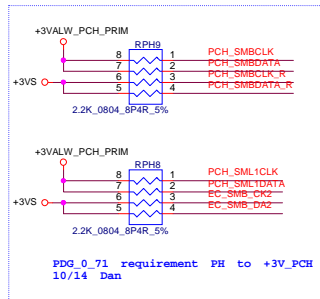
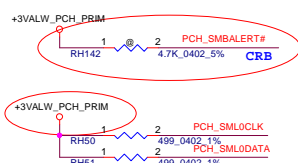
**SPKR / GPP\_B14**  
int. PD  
0 = Disable " Top Swap" mode (Default)  
1 = Enable " Top Swap" mode.

**HDA\_SDO**  
int. PD  
0 = Enable security measures defined in the Flash Descriptor. (Default)  
1 = Disable Flash Descriptor Security (override).

**DDPB\_CTRLDATA / GPP\_I6**  
int. PD  
0 = Port B is not detected. (Default)  
1 = Port B is detected. (Default)

**DDPC\_CTRLDATA / GPP\_I8**  
int. PD  
0 = Port C is not detected. (Default)  
1 = Port C is detected. (Default)

**DDPD\_CTRLDATA / GPP\_I10**  
int. PD  
0 = Port D is not detected. (Default)  
1 = Port D is detected. (Default)



PDG\_0.71 requirement PH to +3V\_PCH 10/14 Dan

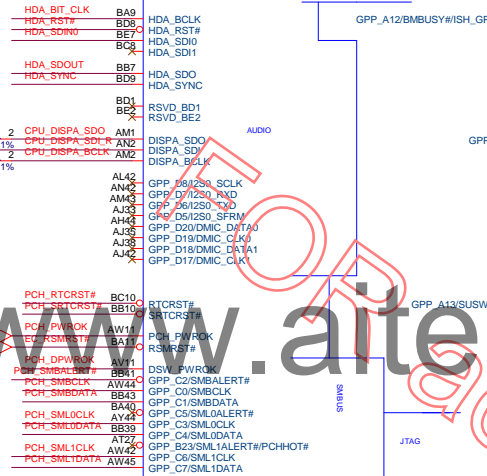
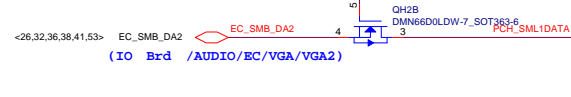
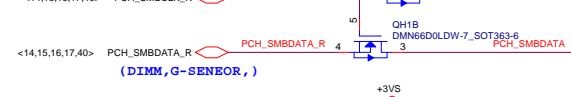
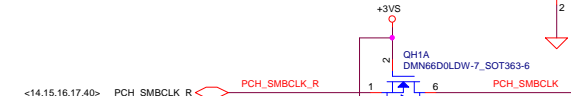
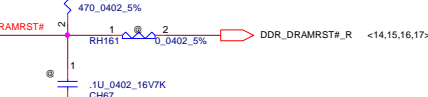
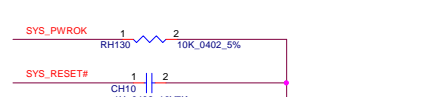
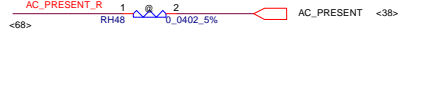
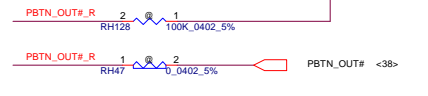
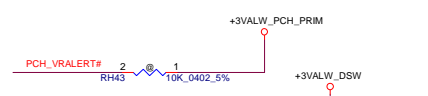
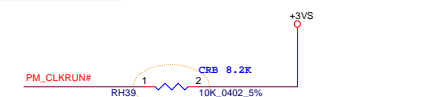


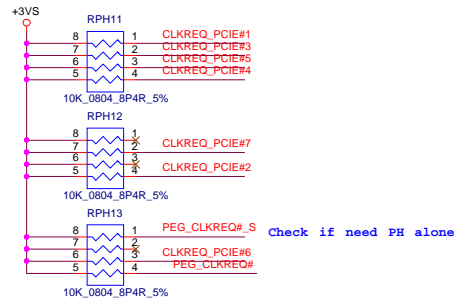
Table 5-10. DDI Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-k $\Omega$ $\pm$ 5% resistor	No Connect
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k $\Omega$ $\pm$ 5% resistor	No Connect
Port 3	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-k $\Omega$ $\pm$ 5% resistor	No Connect

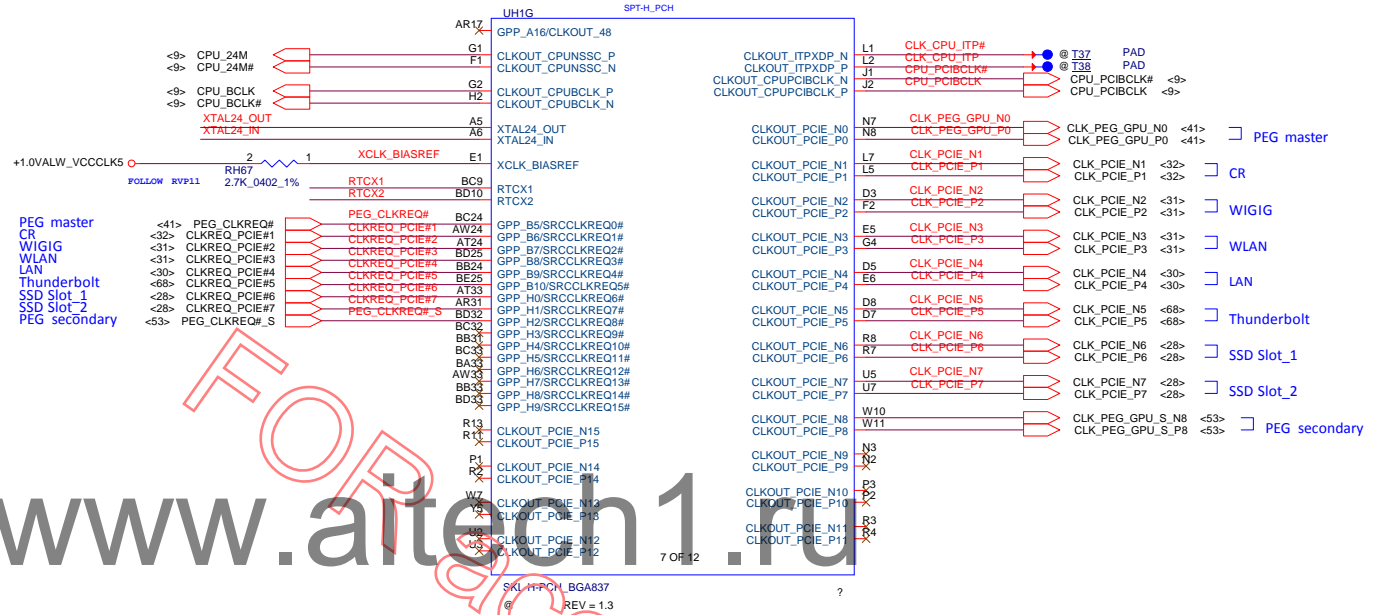
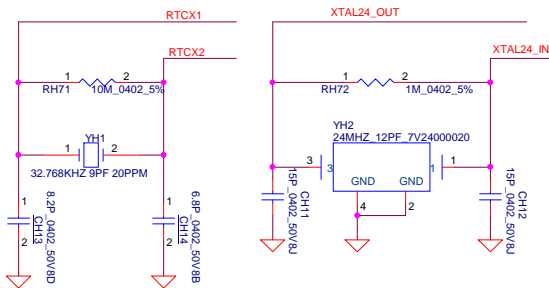


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Follow PDG 0.71Table 52-17  
10/13 Dan  
CHECK NEEDED IF UNUSE?



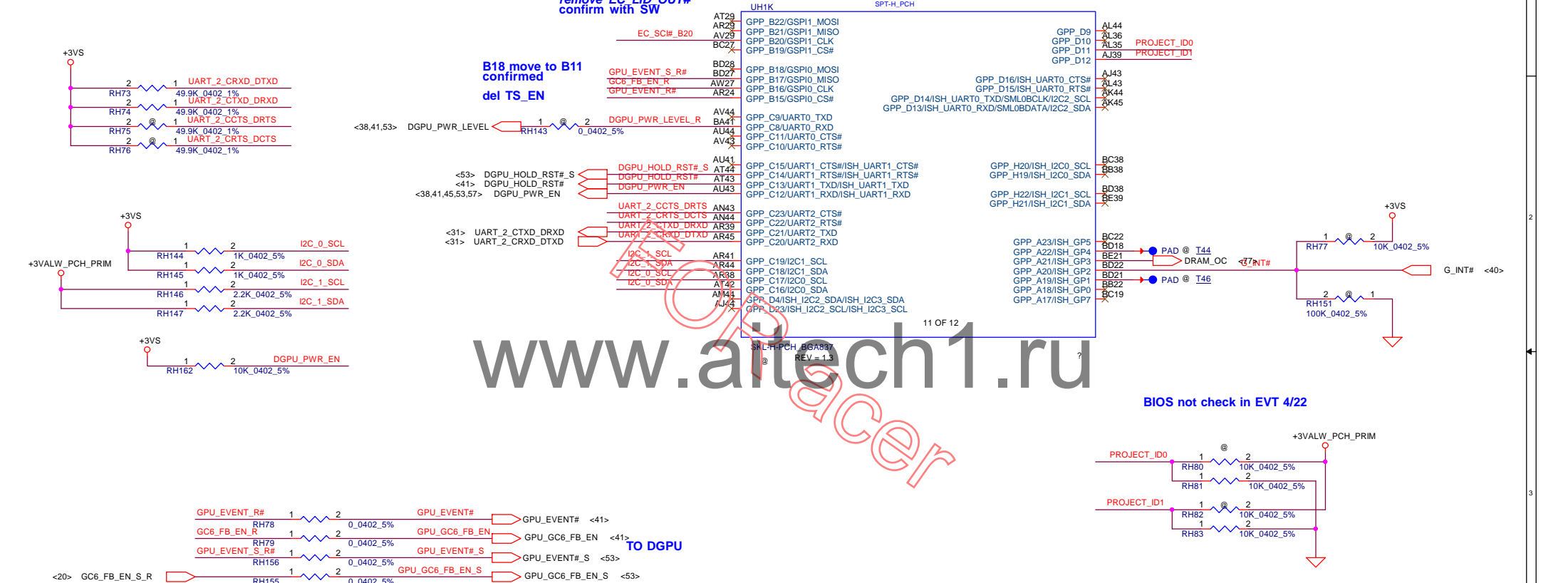
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Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2016/02/01		Deciphered Date		2017/12/31		Title	
										PCH(4/7)CLK	
										C1PR2 LA-E051P	
										Rev 1.0	
										Date: Monday, January 09, 2017	
										Sheet 21 of 103	

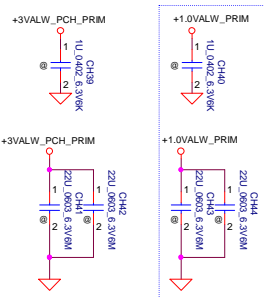
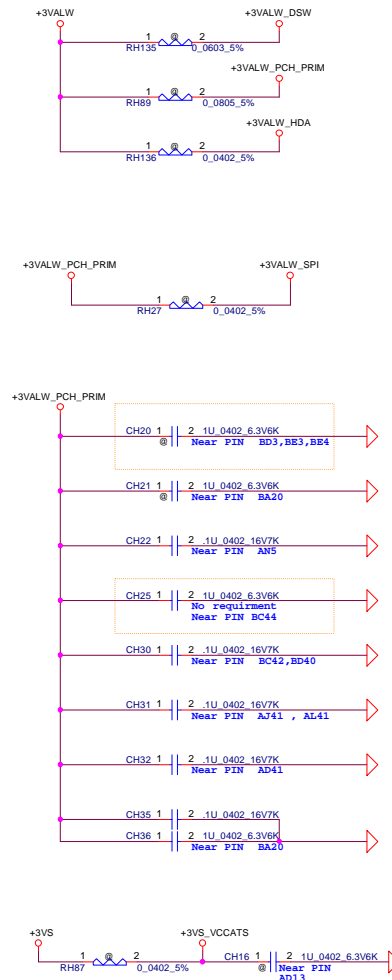
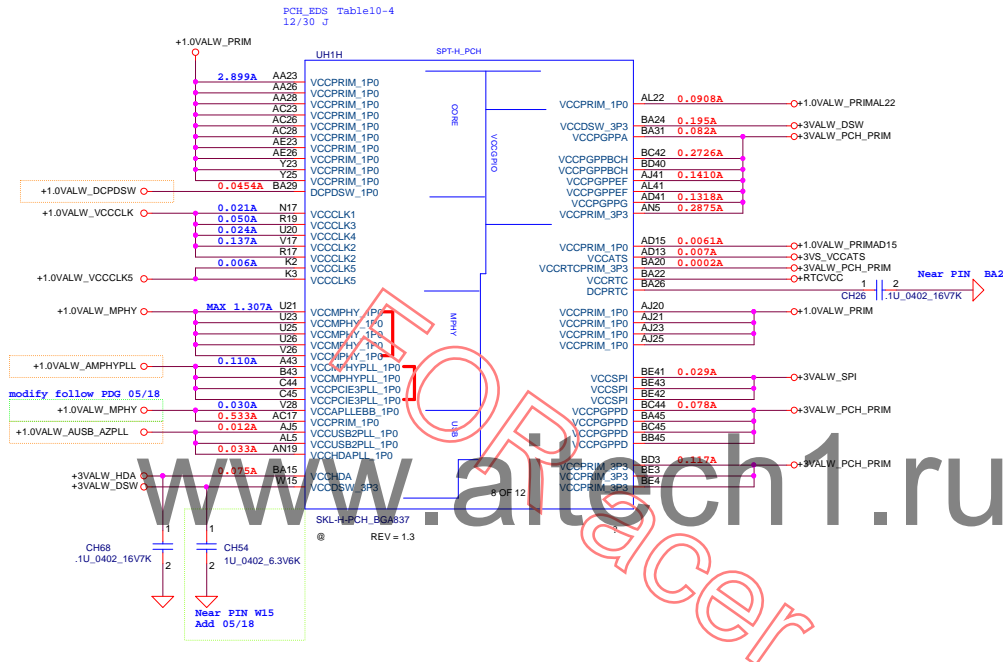
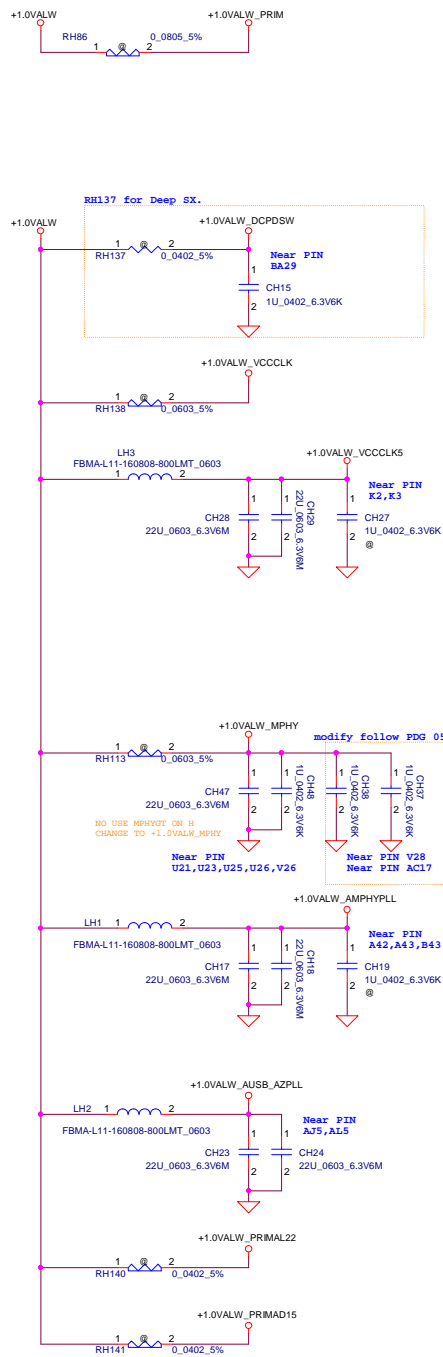
Functional Strap Definitions

**GSPI1\_MOSI / GPP\_B22**  
 int. PD  
 Boot BIOS Destination  
 0 = SPI (Default)  
 1 = LPC

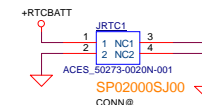
**GSPI0\_MOSI / GPP\_B18**  
 int. PD  
 0 = Disable " No Reboot " mode (Default)  
 1 = Enable " No Reboot " mode (PCH will disable the TCO Timer system reboot feature).



Project ID	Project ID1 GPP_D12	Project ID0 GPP_D11
*C1PR2	0	0
Reserved	0	1
Reserved	1	0
Reserved	1	1

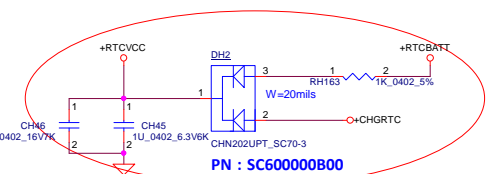


Power Rail	Voltage
+CHGRTC	3.383V(MAX)
BAT54C(VF)	240 mV
+3VL_RTC	3.143V
Result : Pass	

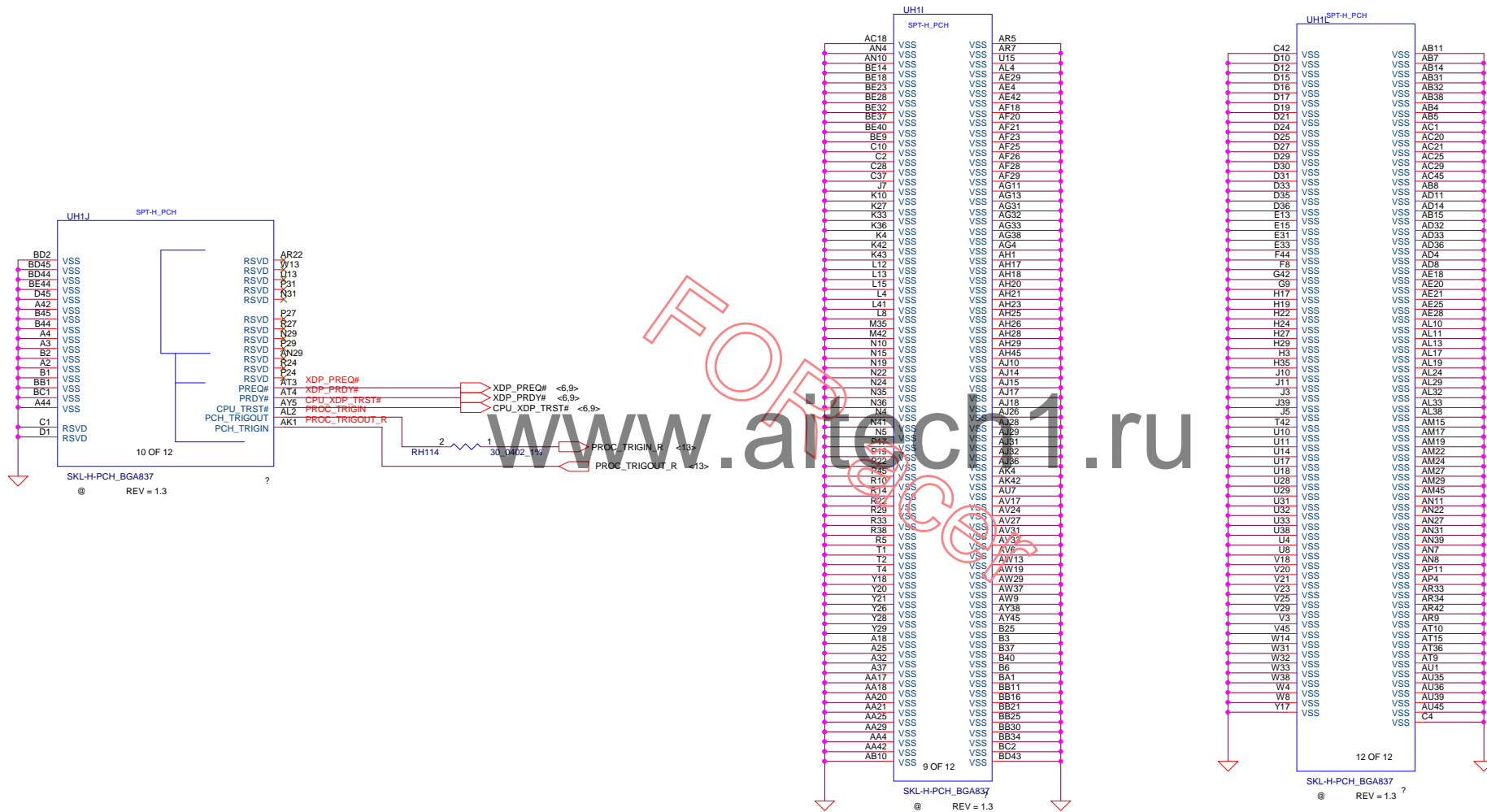


## RTC Battery

Change to non-charge circuit  
DVT 7/11



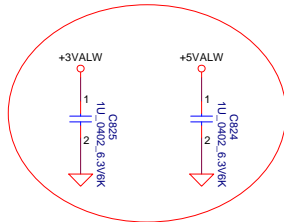
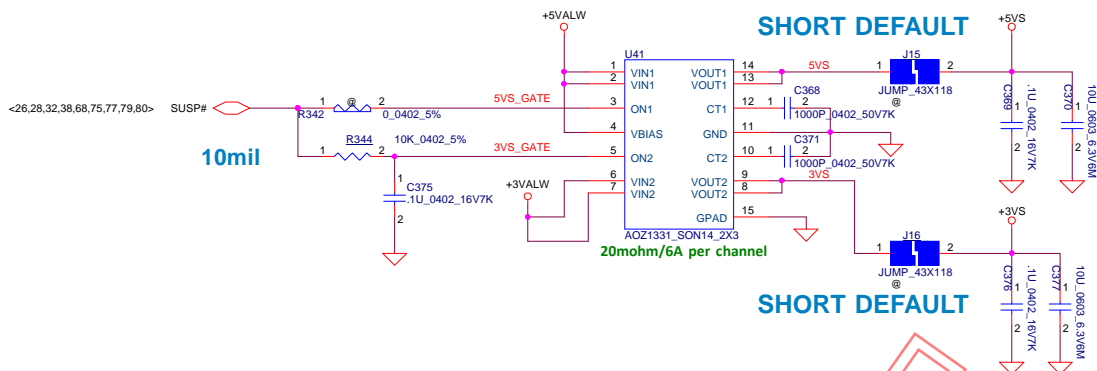
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Issued Date	2016/02/01	Deciphered Date	2017/12/31
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Size	Document Number	Rev	1.0
Customer	C1PR2 LA-E051P	Date	Monday, January 09, 2017
Sheet	23	of	103



Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2016/02/01		Deciphered Date		2017/12/31		Title			
								PCH(7/7)GND			
Size		Document		Number		Rev					
C1PR2		LA-E051P				1.0					
Date:		Monday, January 09, 2017		Sheet		24 of 103					

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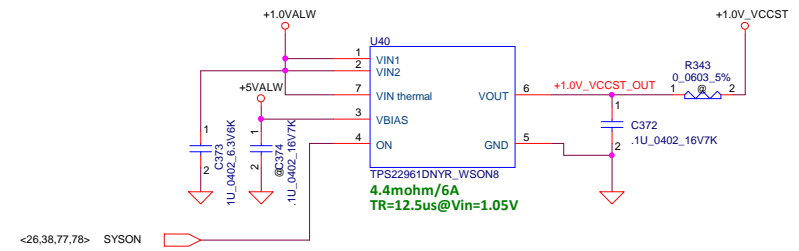
## +5VS and +3VS switch



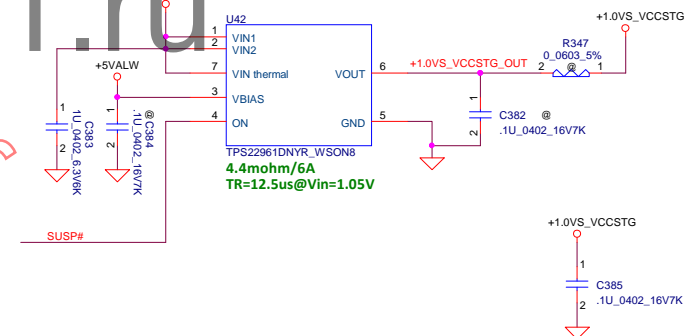
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FOR Pacer

## +1.0VALW TO +1.0V\_VCCST



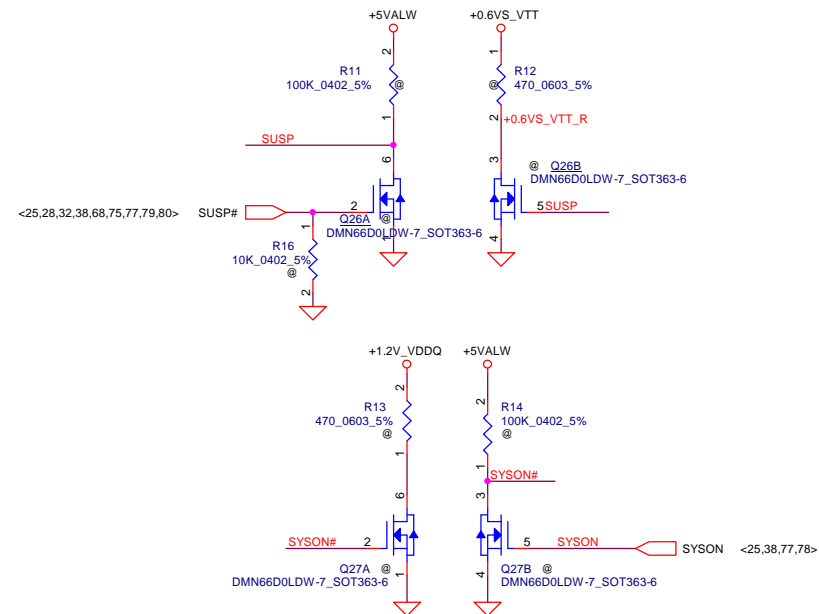
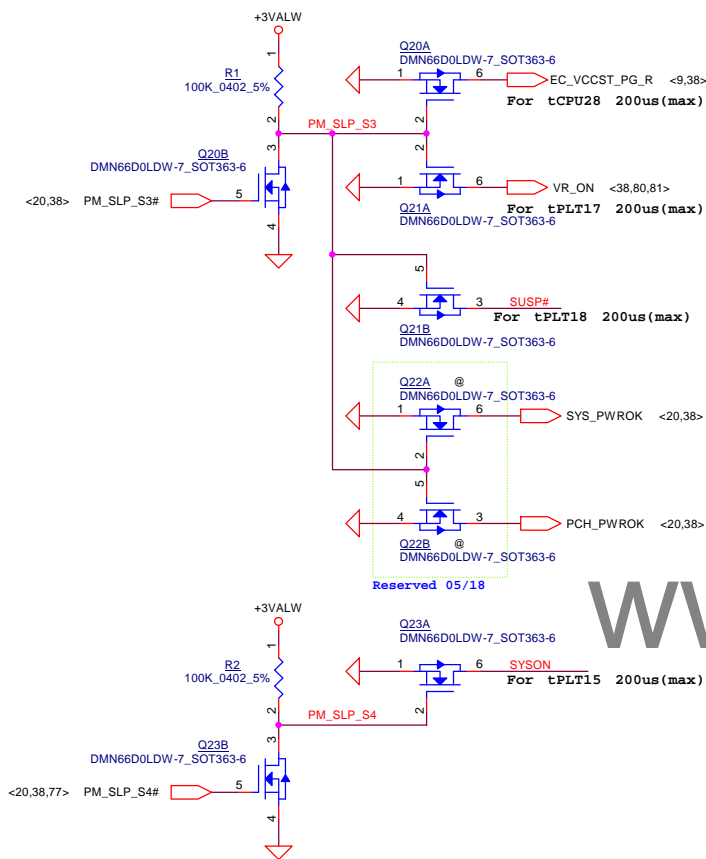
## +1.0VALW TO +1.0VS\_VCCSTG



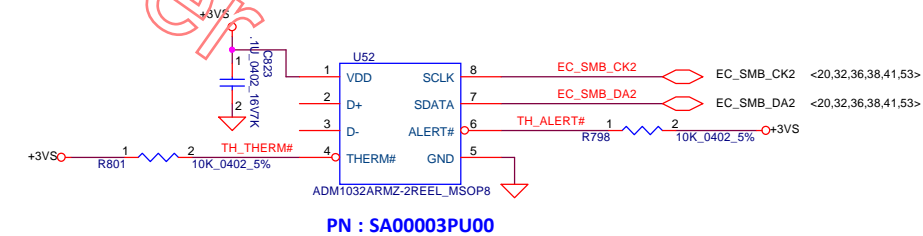
del Load SW for +3VALW\_PCH

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				C1PR2 LA-E051P	
				Date:	Monday, January 09, 2017
				Sheet	25 of 103
				Rev	1.0

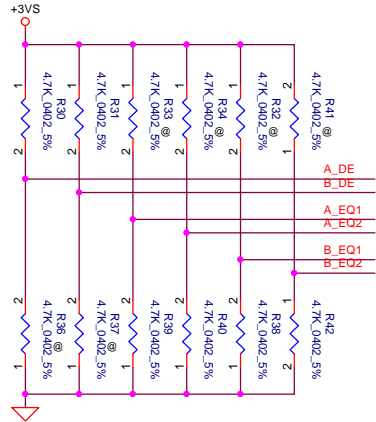
For Power Of f Sequence



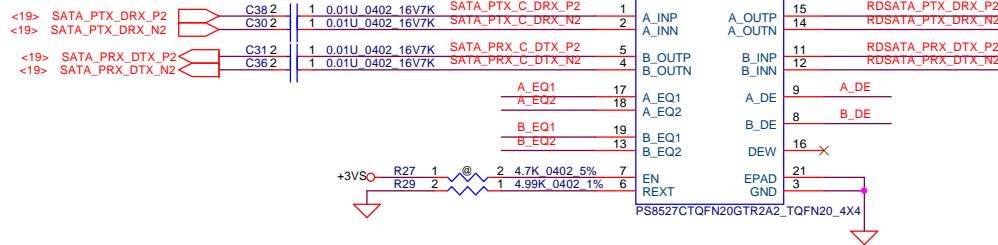
External Thermal Sensor



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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				Custom	CIPR2 LA-E051P
				Date:	Monday, January 09, 2017
				Sheet	26 of 103
				Rev	1.0



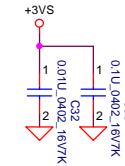
## HDD Re-Driver



De-emphasis width setting for channel A & B .

Internally tied to VDD/2(M status).

DEW	DE pulse duration optimized for
M	SATA 6Gbp/s(default)
L	SATA 6Gbp/s
H	SATA 3Gbp/s



Programmable output de-emphasis level setting for channel A.

Internally tied to VDD/2(M status).

A_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

Programmable output de-emphasis level setting for channel B.

Internally tied to VDD/2(M status).

B_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

Equalizer control and program for channel A.

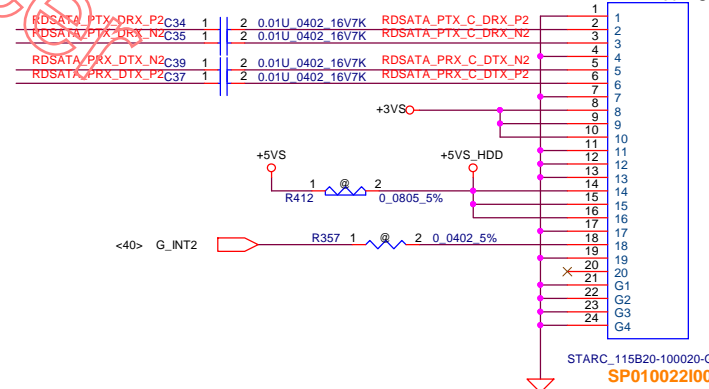
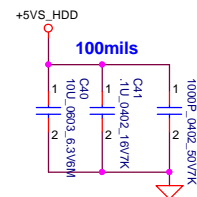
Internally tied to VDD/2 (M status).

A_EQ2	A_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(Default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

Equalizer control and program for channel B.

Internally tied to VDD/2(M status).

B_EQ2	B_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(Default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

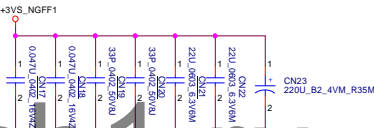
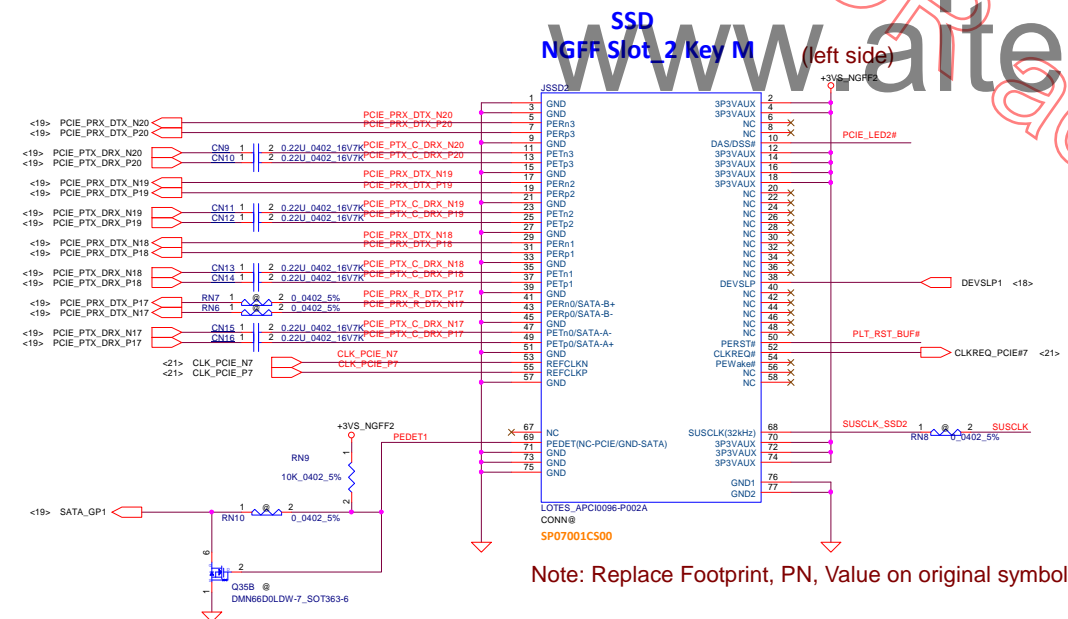
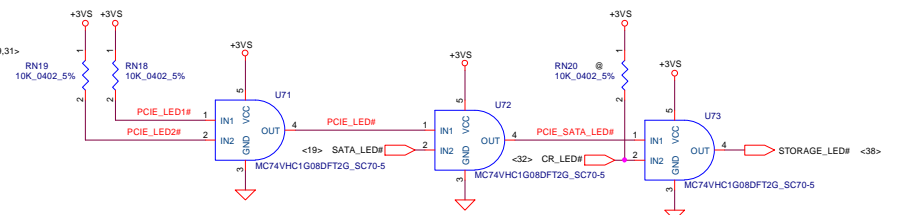
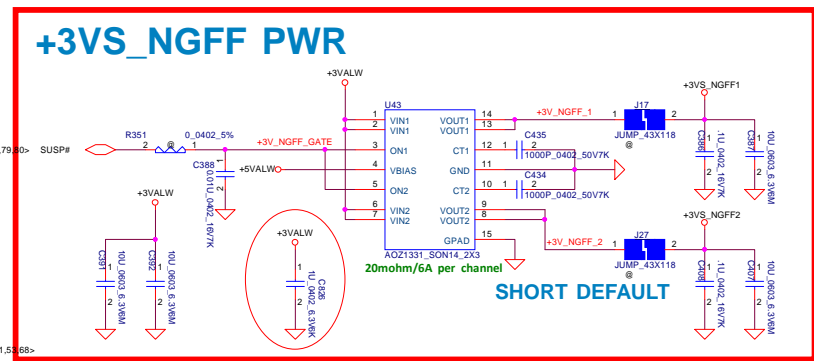
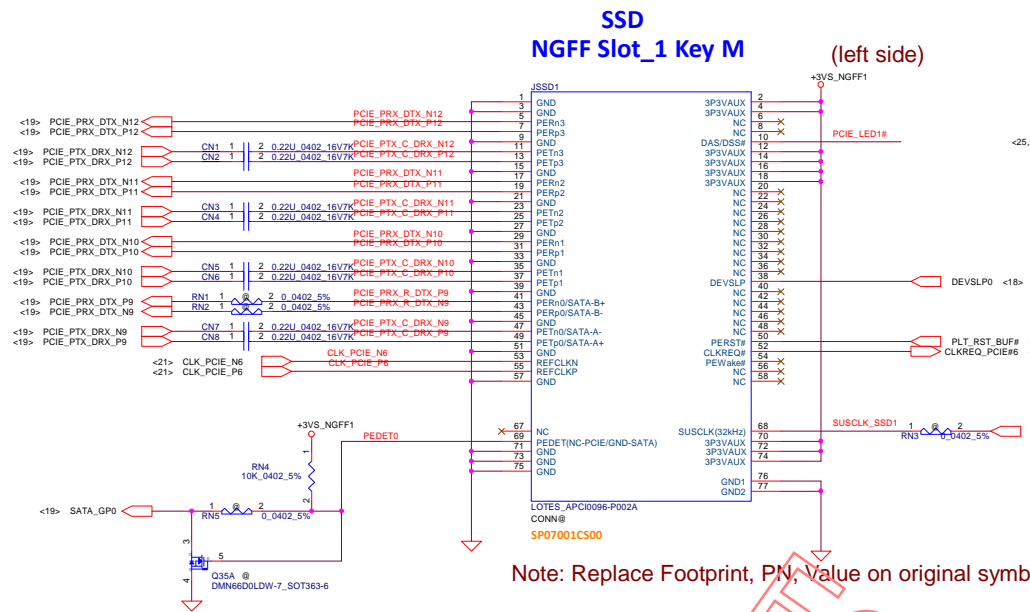


STARC\_115B20-100020-G2-R  
SP010022100

change for DVT

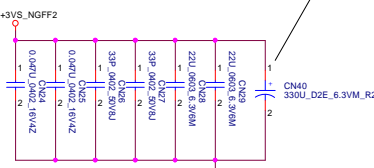
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Size	Custom	Document Number	CIPR2 LA-E051P	Date	Monday, January 09, 2017
Rev	1.0	Sheet	27	of	103





PEDET	Module Type
0	SATA
1	PCIE

placement close PCIE SSD side

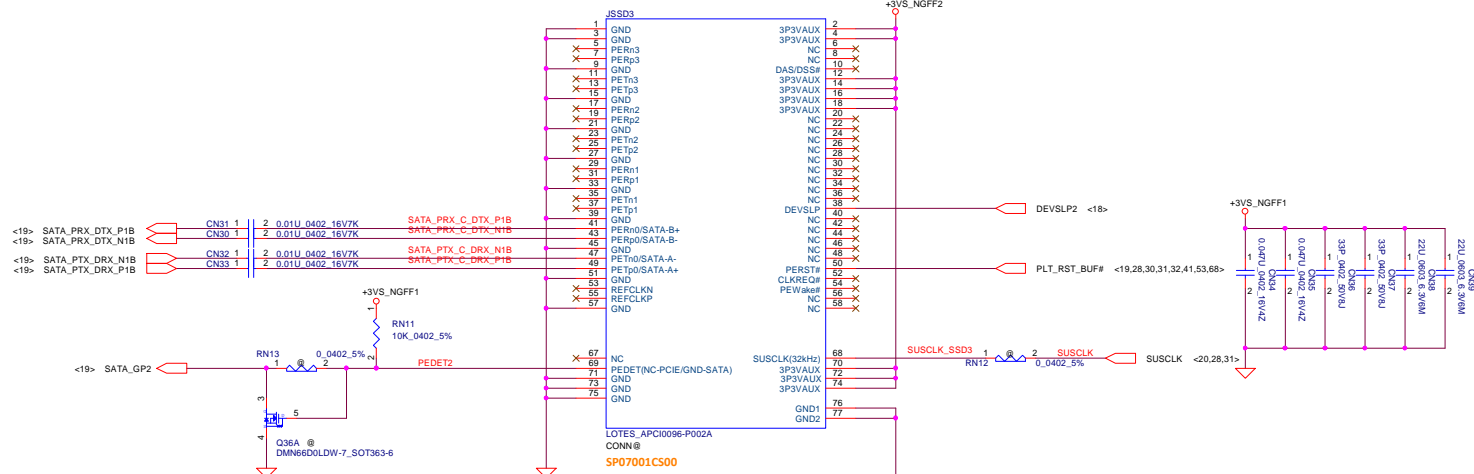


PEDET	Module Type
0	SATA
1	PCIE



# SSD NGFF Slot\_3 Key M

(right side)

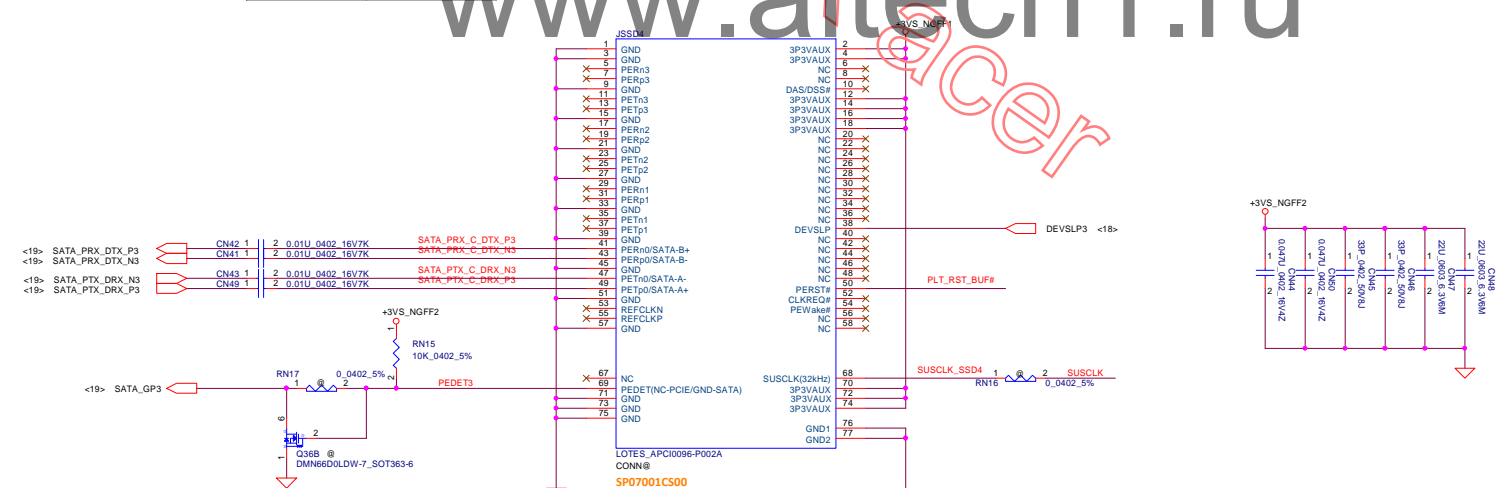


Note: Replace Footprint, PN, Value on original symbol

PEDET	Module Type
0	SATA
1	PCIE

# SSD NGFF Slot\_4 Key M

(right side)



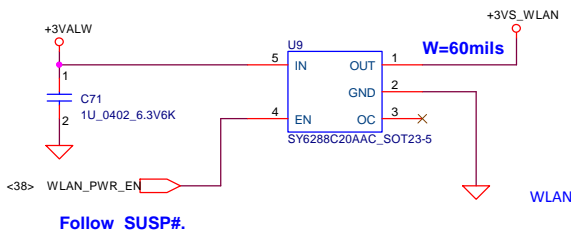
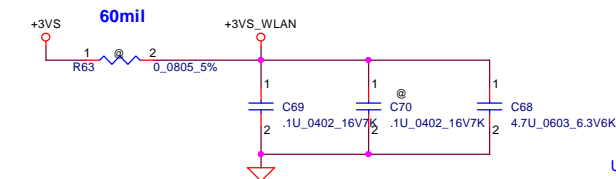
Note: Replace Footprint, PN, Value on original symbol

PEDET	Module Type
0	SATA
1	PCIE

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				Date	Monday, January 09, 2017
				Sheet	29 of 103
				Rev	1.0

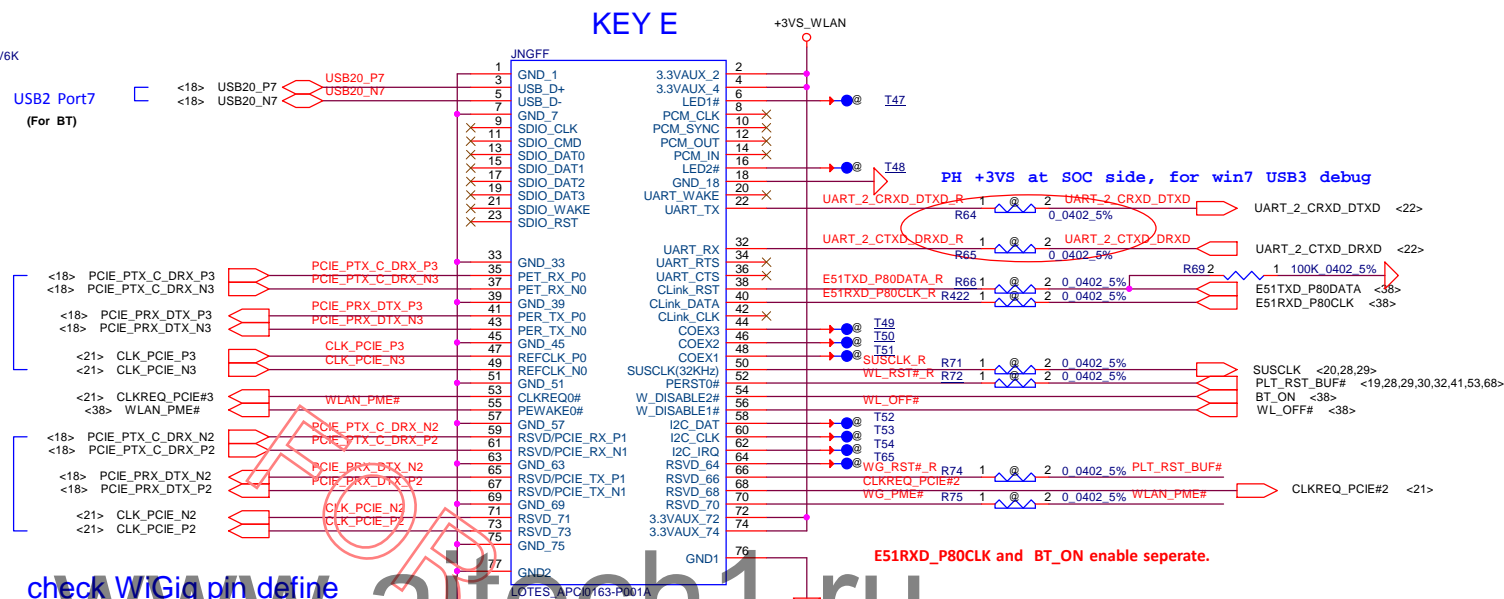


## Wireless LAN



### WiGig/WLAN/BT Combo Host Pin Configuration

W0096	Pin#	Standard Definition	M.2 CONNECTOR	Standard Definition	Pin#	W0096
				GND	75	GND
VCCD_3V3	74	3.3V		REFCLKN1	73	11ad PE REFCLKP
VCCD_3V3	72	3.3V		REFCLKP1	71	11ad PE REFCLKP
11ad PE WAKEN	70	PEWAKE1#		GND	69	GND
11ad PE CLKREQN	68	CLKREQ0#		PETn1	67	11ad PE TXP0
11ad PE PERSTN	66	PERST1#		PETp1	65	11ad PE TXN0
11ad JTMS	64	Reserved		GND	63	GND
11ad JTDI	62	ALERT#		PERn1	61	11ad PE RXP0
11ad JTDO	60	I2C CLK		PERp1	59	11ad PE RXN0
11ad JTCK	58	I2C DATA		GND	57	GND
EDGE_WDISABLEN1*	56	W_DISABLE1#		PEWAKE0#	55	11ac PE WAKEN
EDGE_WDISABLEN2*	54	W_DISABLE2#		CLKREQ0#	53	11ac PE CLKREQN
11ac PE PERSTN	52	PERST0#		GND	51	GND
SUSCLK	50	SUSCLK(32kHz)		REFCLKN0	49	11ac PE REFCLKN
NC	48	COEX1		REFCLKP0	47	11ac PE REFCLKP
NC	46	COEX2		GND	45	GND
NC	44	COEX3		PETn0	43	11ac PE TXN
11ad PE RXP1**	42	Reserved		PETp0	41	11ac PE TXP
11ad PE RXN1**	40	Reserved		GND	39	GND
GND	38	Reserved		PERn0	37	11ac PE RXN
11ad PE TXP1**	36	N/C		PERp0	35	11ac PE RXP
11ad PE TXN1**	34	N/C		GND	33	GND
GND	32	N/C		NOTCH		NOTCH
NOTCH		NOTCH		NOTCH		NOTCH
NOTCH		NOTCH		NOTCH		NOTCH
NOTCH		NOTCH		NOTCH		NOTCH
NOTCH		NOTCH		N/C	23	NC
11ad JT_RST	22	N/C		N/C	21	NC
NC	20	N/C		N/C	19	NC
GND	18	GND		N/C	17	NC
EDGE_LED2*	16	LED2#		NOTCH		NOTCH
NOTCH		NOTCH		NOTCH		NOTCH
NOTCH		NOTCH		NOTCH		NOTCH
NOTCH		NOTCH		NOTCH		NOTCH
NOTCH		NOTCH		GND	7	GND
EDGE_LED1*	6	LED1#		USB_D-	5	11ac USB DNEG
VCCD_3V3	4	3.3V		USB_D+	3	11ac USB DPOS
VCCD_3V3	2	3.3V		GND	1	GND



check WiGig pin define

NGFF WL+BT (KEY E)  
WiGig

Note: Replace Footprint, PN, Value on original symbol

### 3.1.8.1.3.1.7.1. UART Wakeup

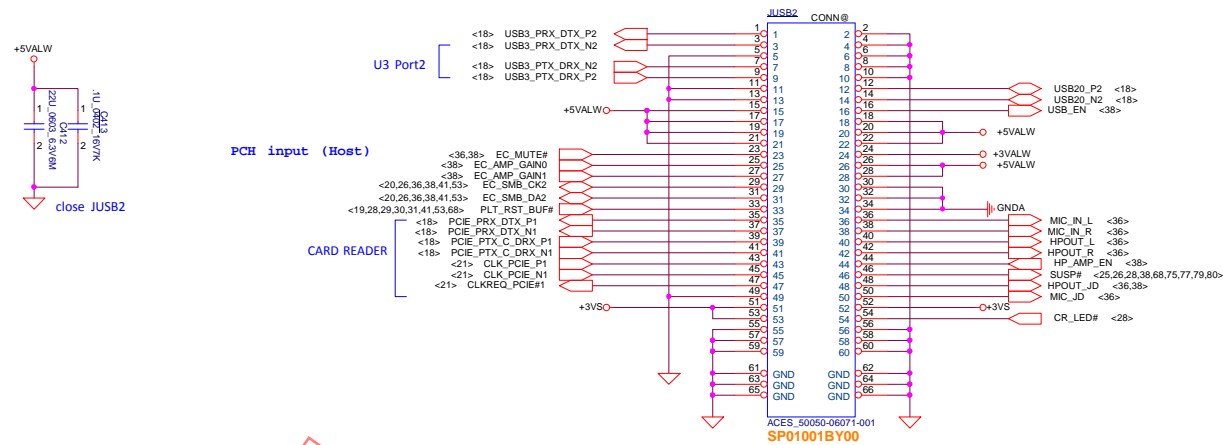
The UART power management protocol supports the following 4-wire and 5-wire interfaces:

- **RDX** **UART** **RXD** (Input): Receive Data
- **RTX** **UART** **TXD** (Output): Transmit Data
- **UART** **RTS** (Input): Request to Send (Host Flow Control)
- **UART** **CTS** (Output): Clear to Send (Device Flow Control)
- **Host Wake Up** **UART** **Wake#** (Output): Host wake-up line is optional in case the host support in hand wake-up

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				Size	Document Number
				Custom	<b>CIPR2 LA-E051P</b>
Date: Monday, January 09, 2017				Sheet	31 of 103
				Rev	1.0

USB3.0 I/O & SUB/B

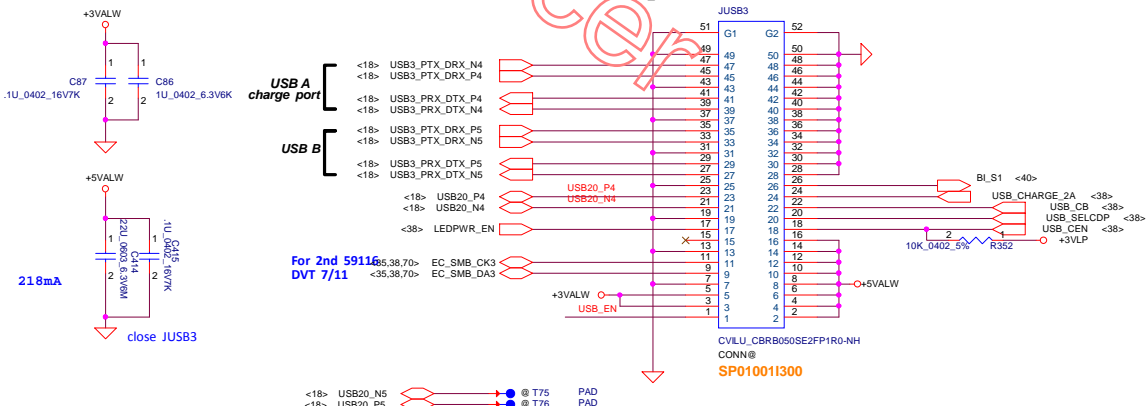
60pin I/O Conn.



USB SUB/B CONN

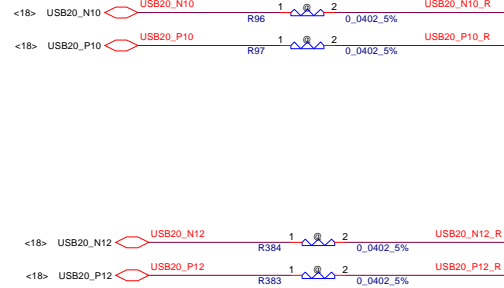
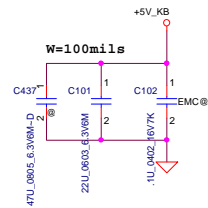
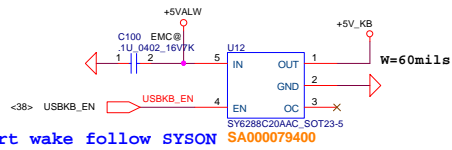
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50pin USB3 Conn.

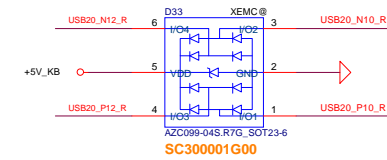
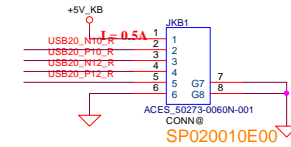


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				Size	Document Number
				Custom	CIPR2 LA-E051P
				Date:	Monday, January 09, 2017
				Sheet	32 of 103
				Rev	1.0

## INT\_KBD Conn.

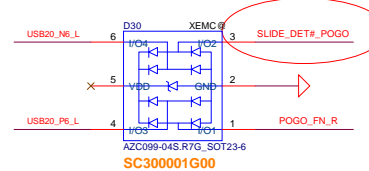
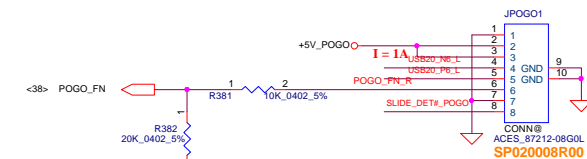
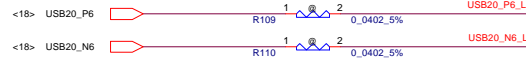
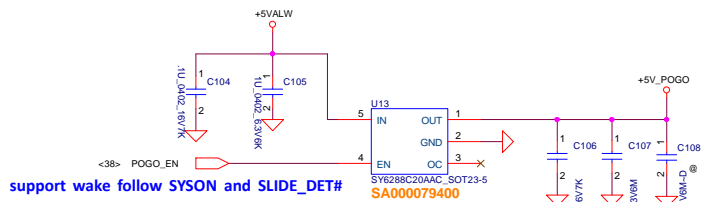


### 1A\_check spec



add for KB BL

## Touch PAD use POGO design



checked 3/15

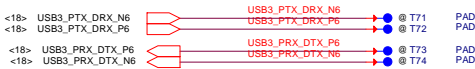
	High	Low
POGO_FN	Touch pad	number key

Un-plug is low.

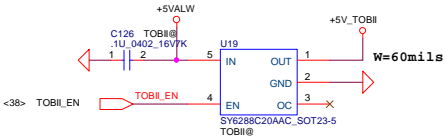
Gnd/Vbus/D-/D+/Det/Gnd \_ module side pindefine

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Custom	Monday, January 09, 2017	Sheet	33	of 103

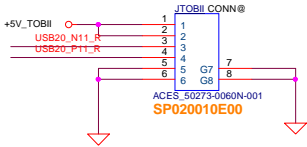
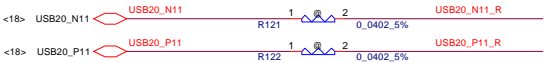
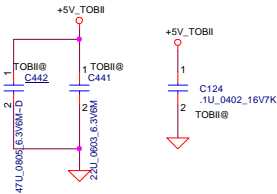
3D CAMERA



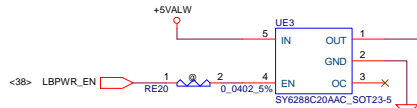
Tobii Eye Tracker



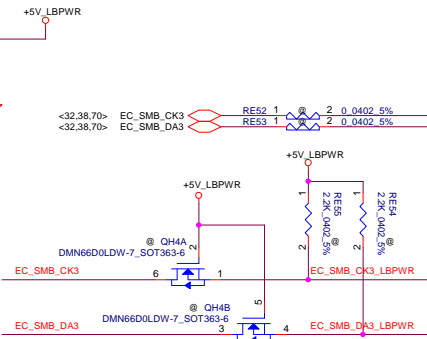
follow SUSP#



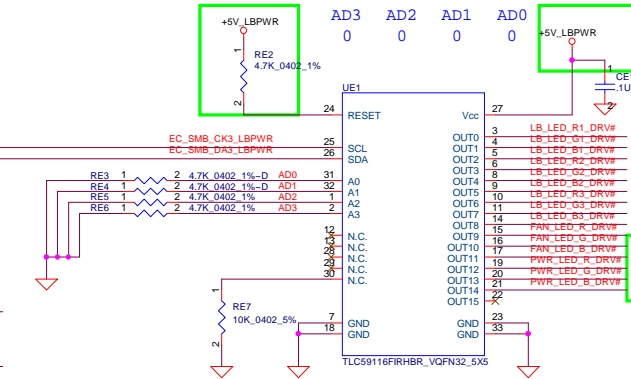
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Issued Date	2016/02/01	Deciphered Date	2017/12/31	Title		
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				Custom	CIPR2 LA-E051P	1.0
Date:				Monday, January 09, 2017		
				Sheet	34	of 103



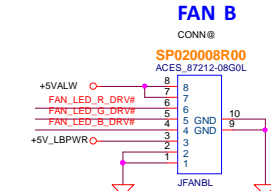
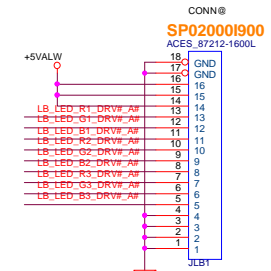
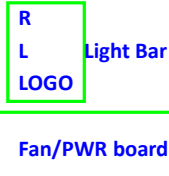
follow SYSON



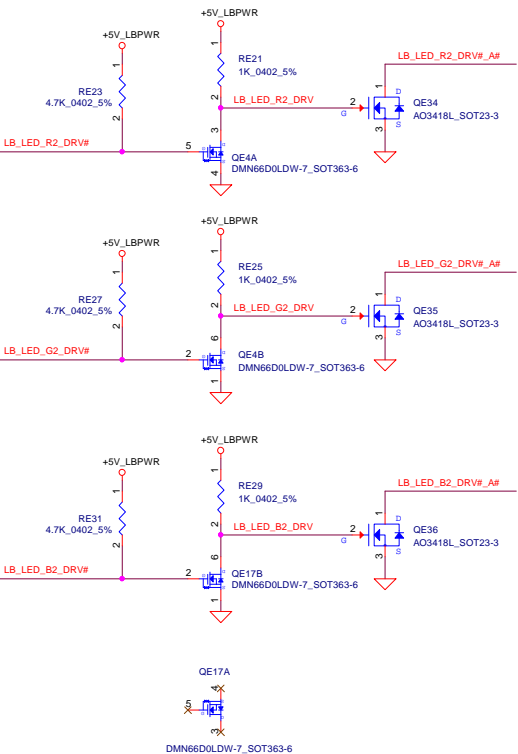
default bypass



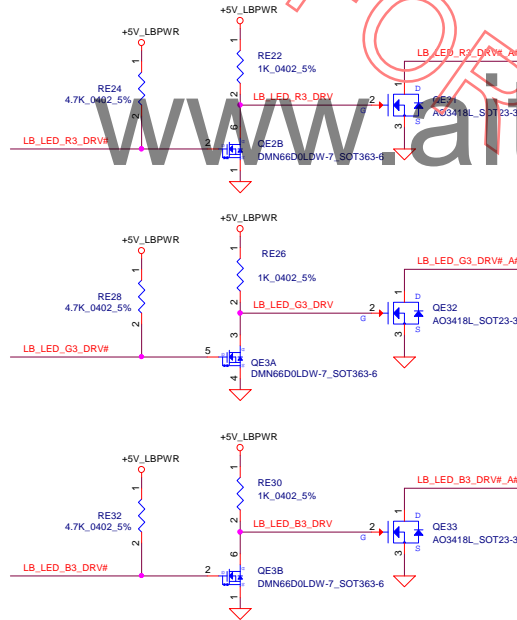
set RE7 to 10k / output = 1.875mA



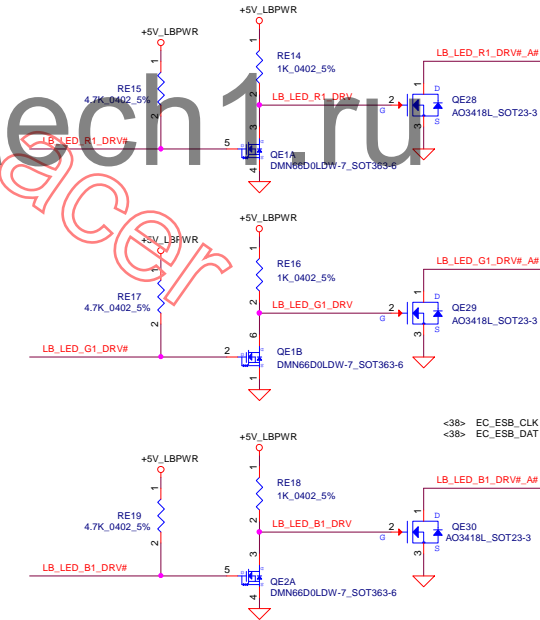
### L Light Bar Backlight



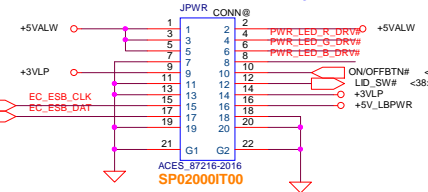
### LOGO Backlight



### R Light Bar Backlight

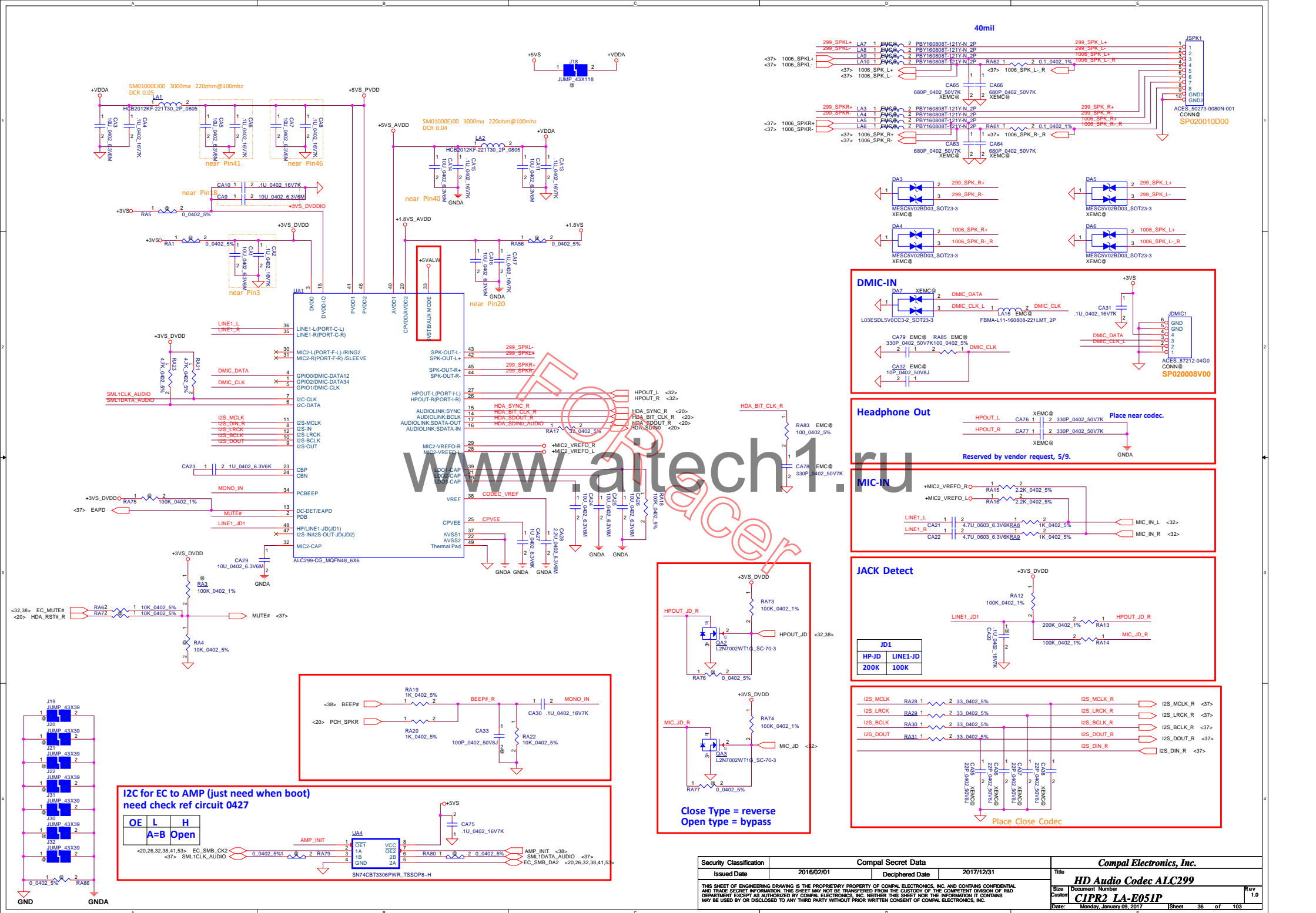


### PWR B / Marco Key



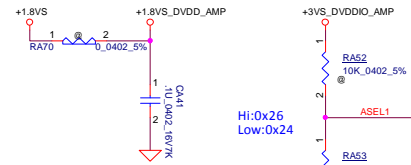
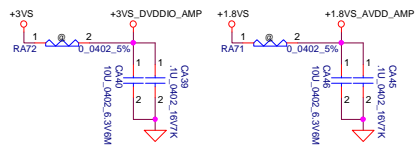
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				C1PR2 LA-E051P				1.0			
Date: Monday, January 09, 2017				Sheet 35 of 103							





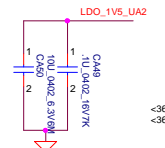


## For SPK Conn.

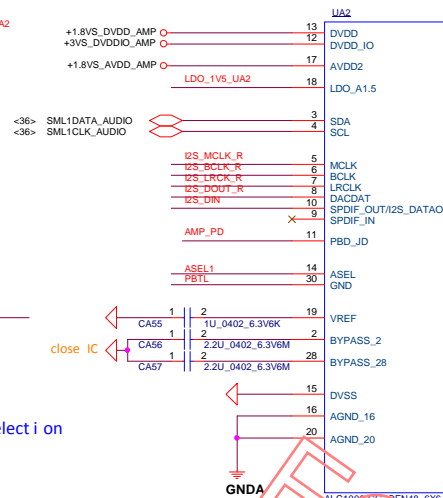
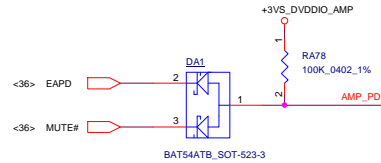


Hi:0x26  
Low:0x24

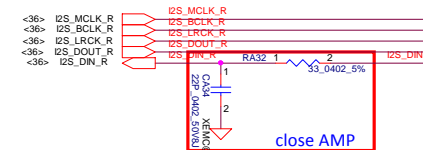
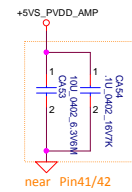
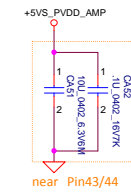
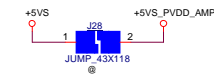
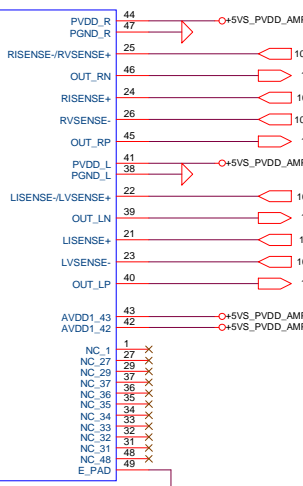
Address Set ti ng  
Low:0x24



Output Mode Select i on  
Low:BT L  
Hi:PBTL

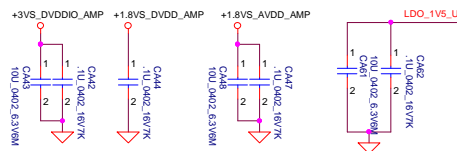


ASK vendor for sense pin connect i on



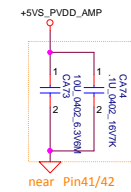
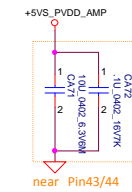
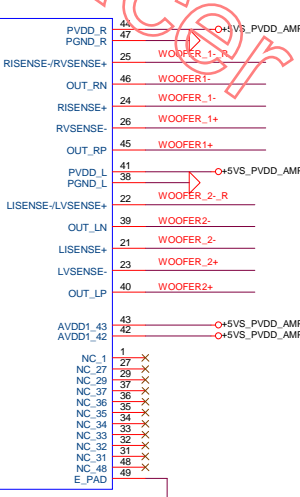
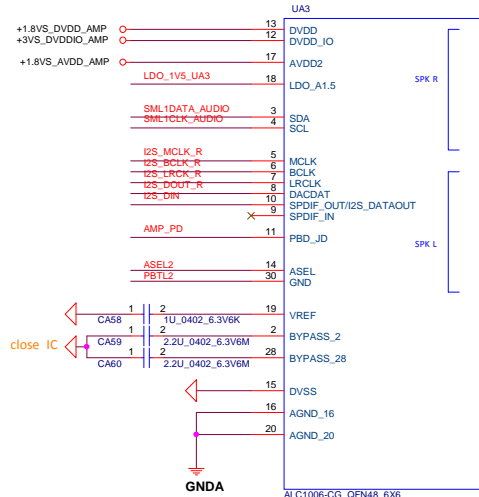
www.aitech1.ru

For woofer Conn.

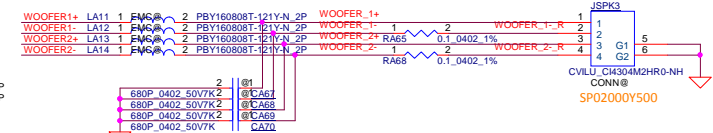


Address Set ti ng  
Hi:0x26

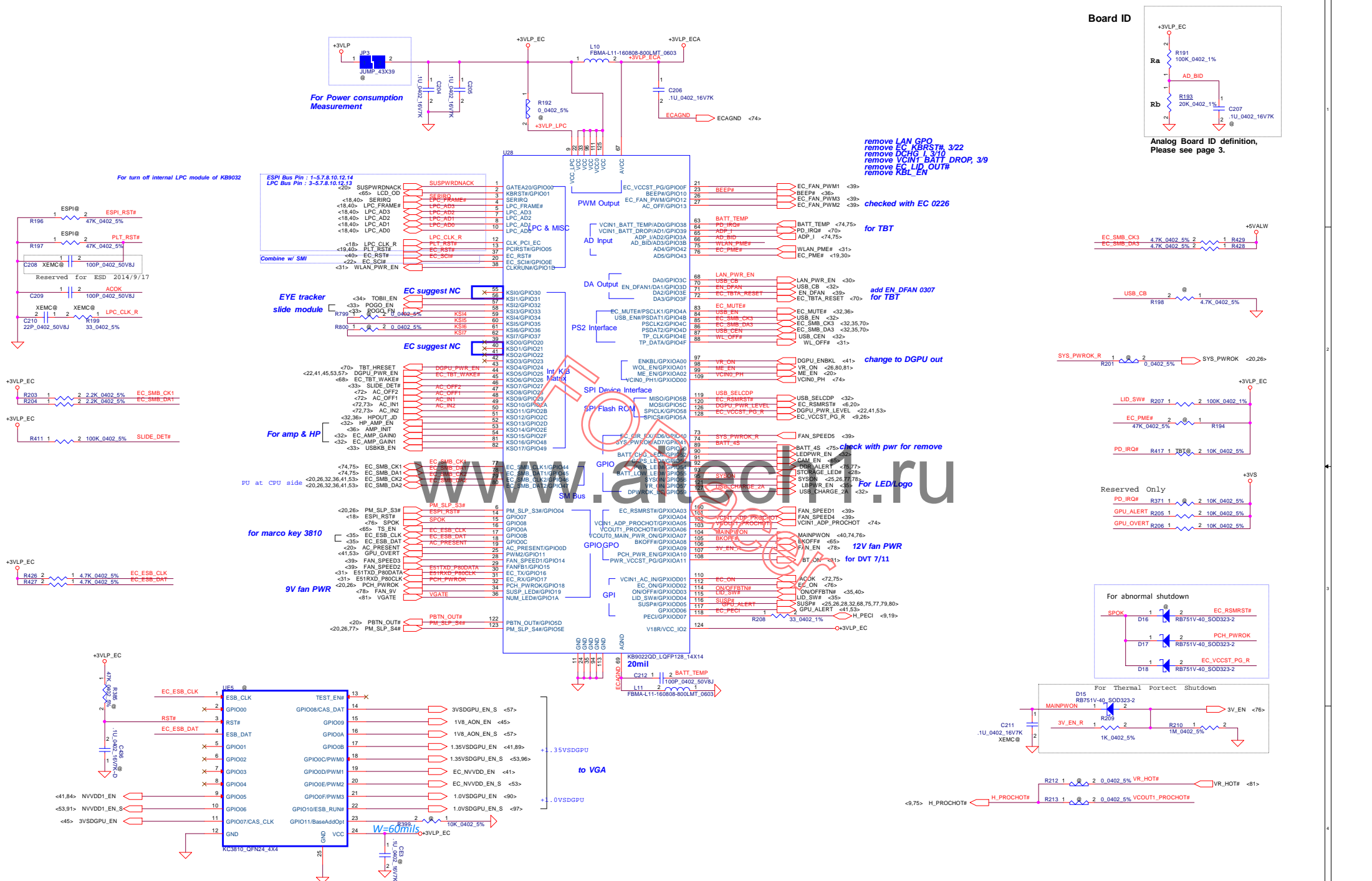
Output Mode Select i on  
Low:BT L  
Hi:PBTL



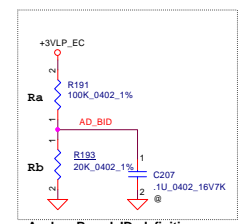
Subwoofer Conn.



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				Size	Document Number
				Custom	CIPR2 LA-E051P
				Date:	Monday, January 09, 2017
				Sheet	37 of 103
				Rev	1.0



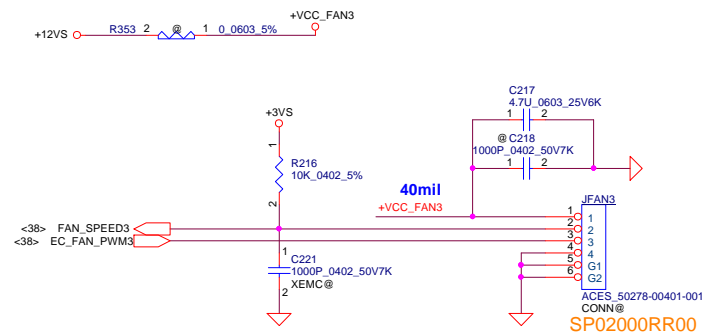
Board ID



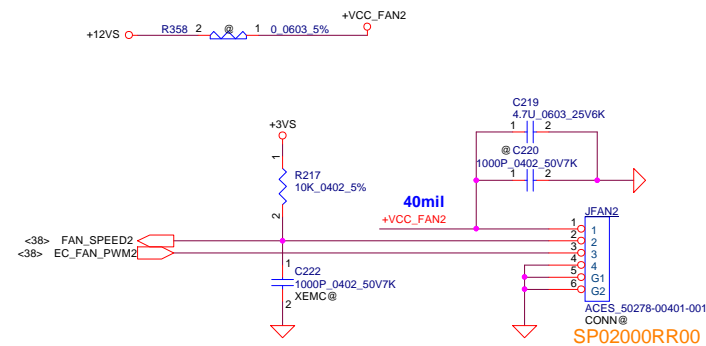
Analog Board ID definition, Please see page 3.

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				Custodian	CIPR2 LA-E051P
				Date	Monday, January 09, 2017
				Sheet	38 of 103

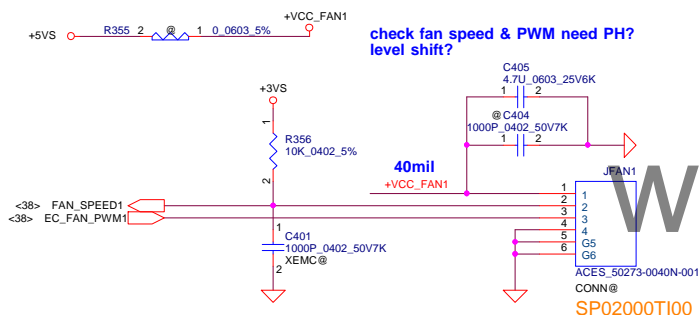
### FAN Control circuit-1 (Left)



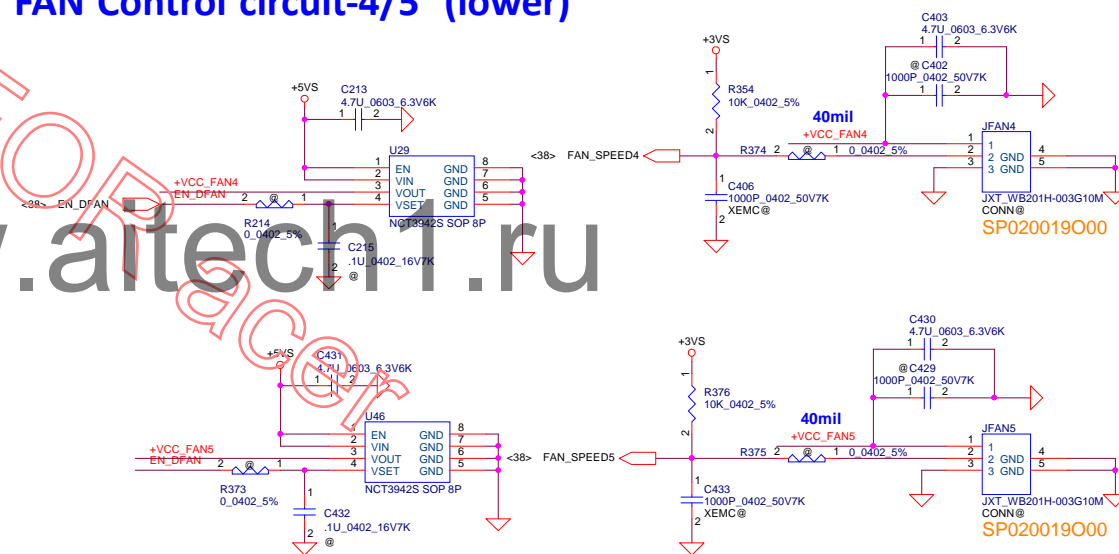
### FAN Control circuit-2 (Right)



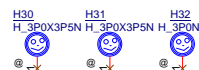
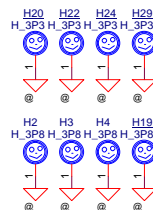
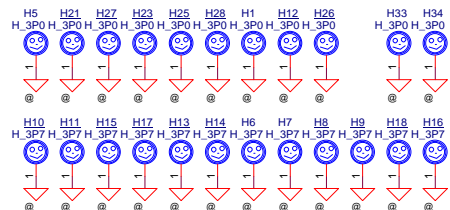
### FAN Control circuit-3 (Center)



### FAN Control circuit-4/5 (lower)

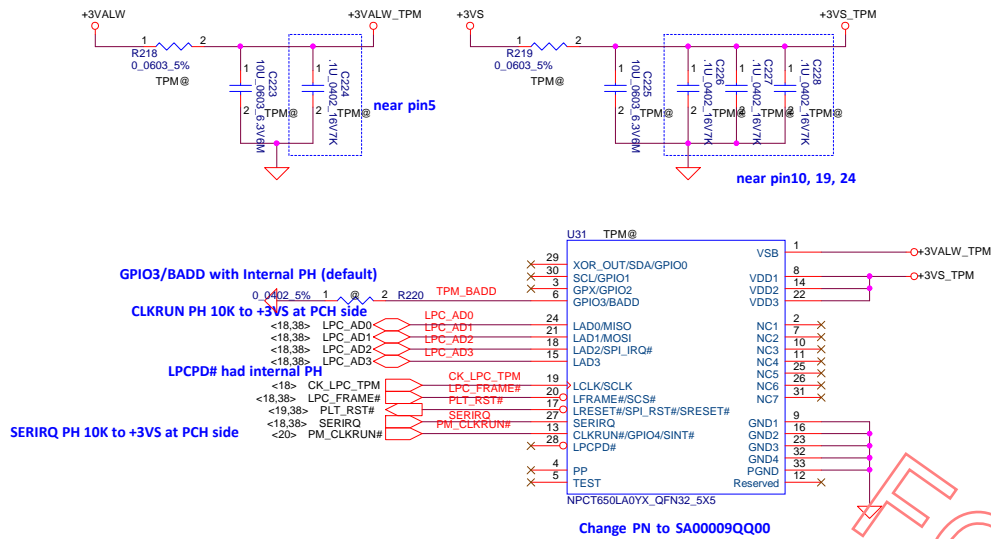


## Screw Hole

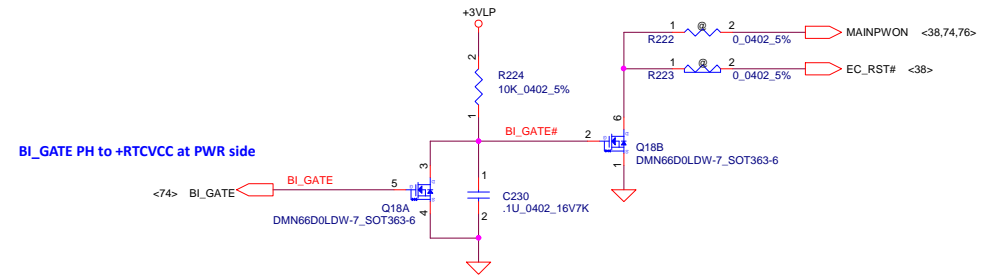


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					<b>CIPR2 LA-E051P</b>	1.0
				Date:	Monday, January 09, 2017	Sheet 39 of 103

# TPM Board for 2016



# Reset Circuit



# BI SW

BI SW (Bot)

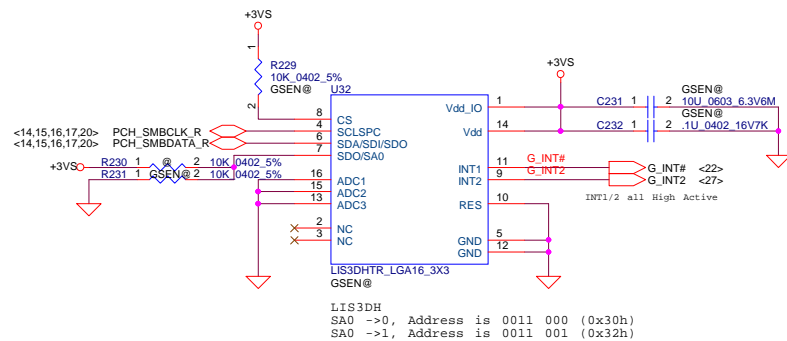
BI SW (Top)

Reset BTN

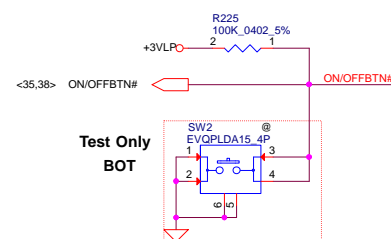
move to pwr/b



# reserve G-Sensor



# ON/OFF BTN

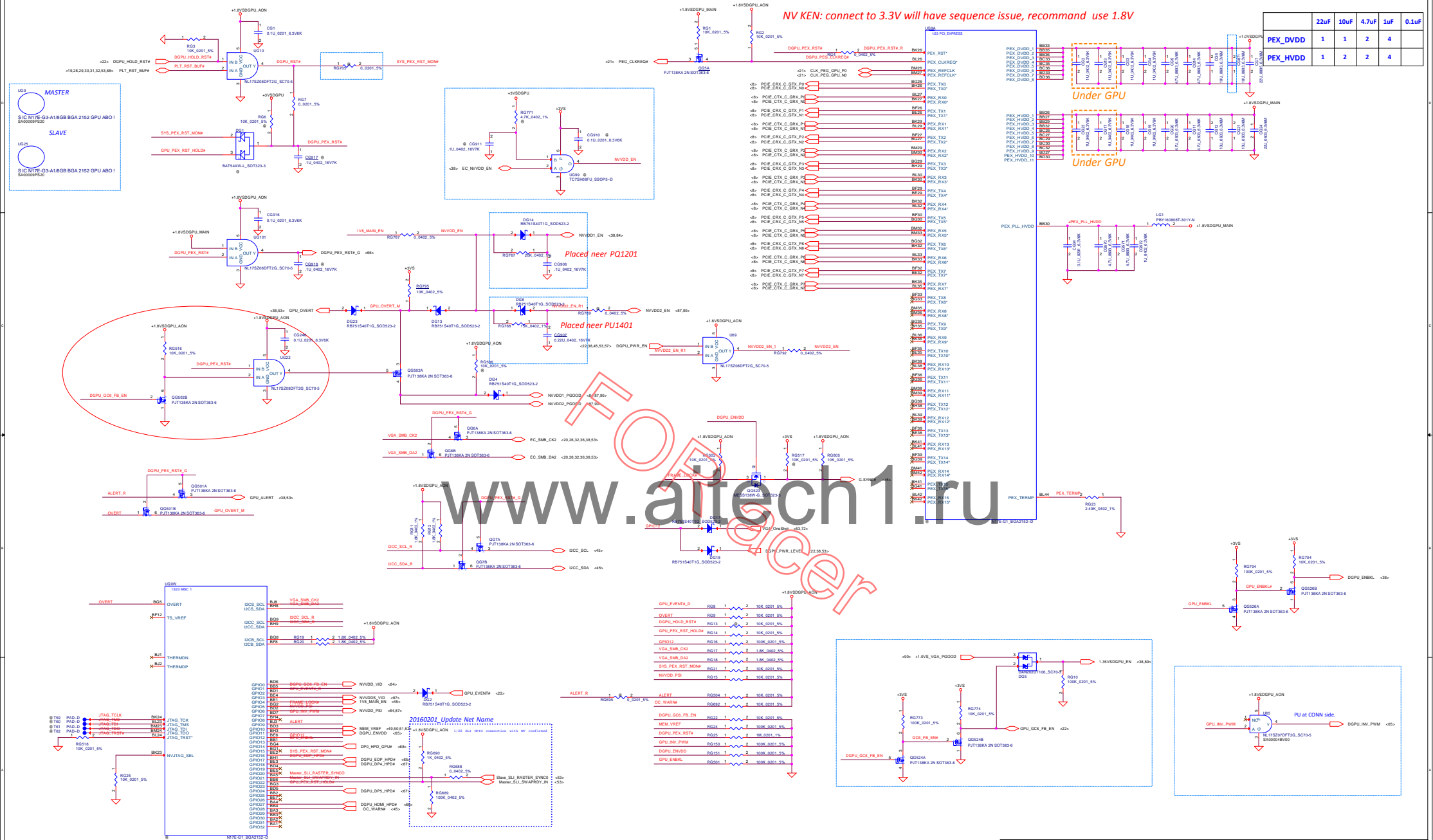


**Move Lid Switch to JPWR**

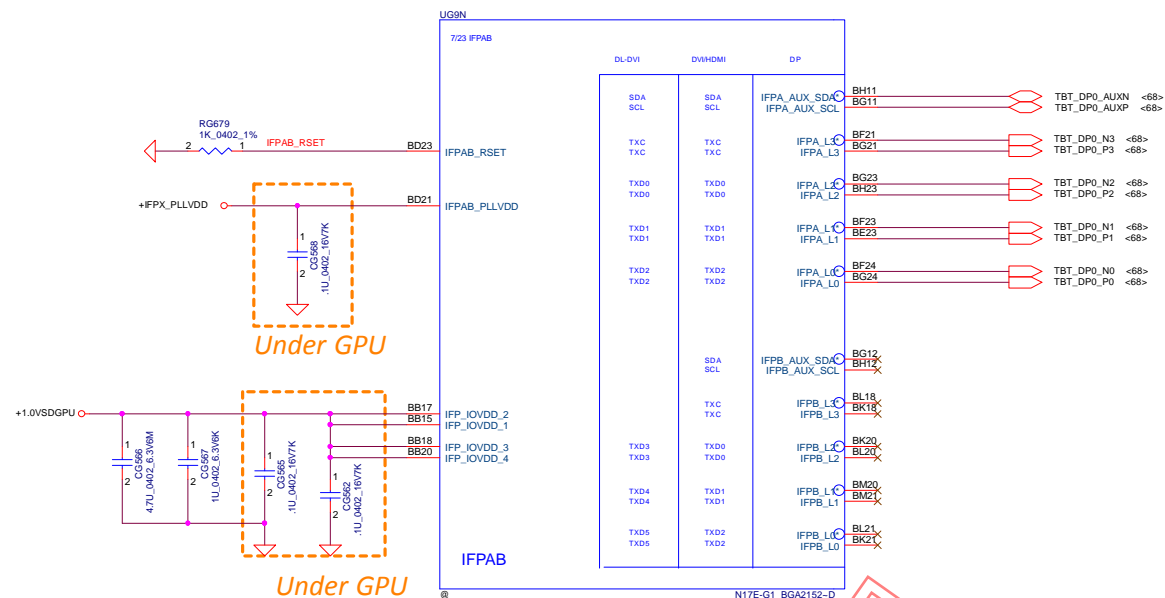
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Issued Date	2016/02/01	Deciphered Date	2017/12/31	Title	
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Size		Document Number		Rev	
Custort		CIPR2 LA-E051P		1.0	
Date:		Monday, January 09, 2017		Sheet 40 of 103	

NV KEN: connect to 3.3V will have sequence issue, recommend use 1.8V

	22uF	10uF	4.7uF	1uF	0.1uF
PEX_DVDD	1	1	2	4	
PEX_HVDD	1	2	2	4	

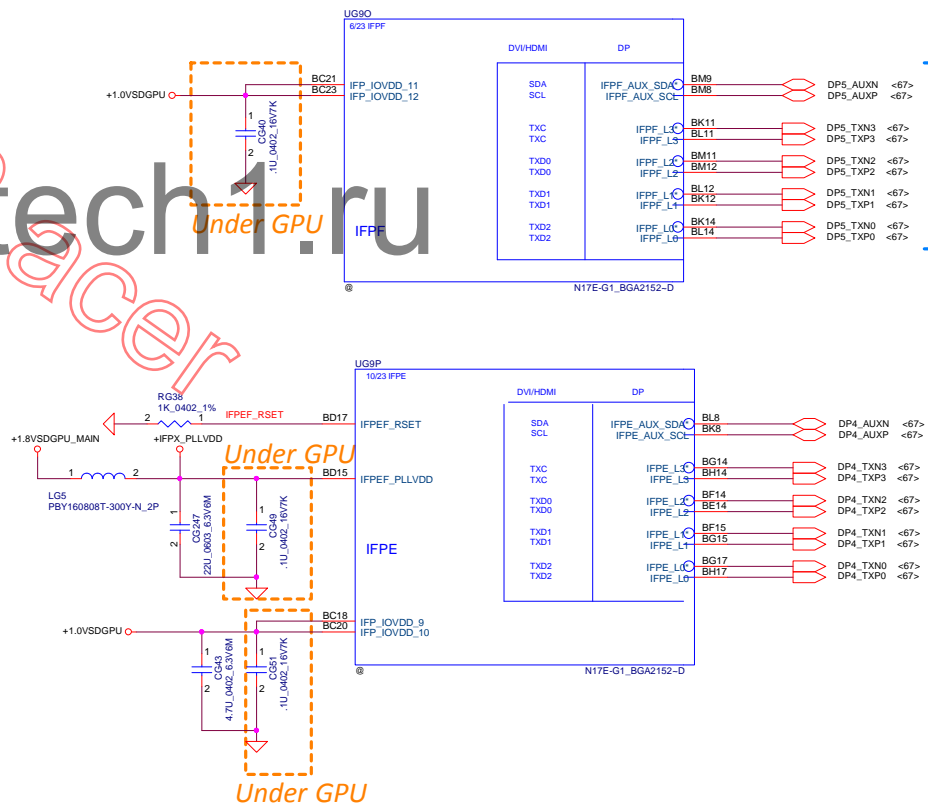


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Issued Date	2016/03/01	Designated Date	2017/12/21
Doc No.	N17E-G1(I/6) PCIe GPIO-M		
Rev.	CIPR2 LA-E051P		
Page	1	1	1



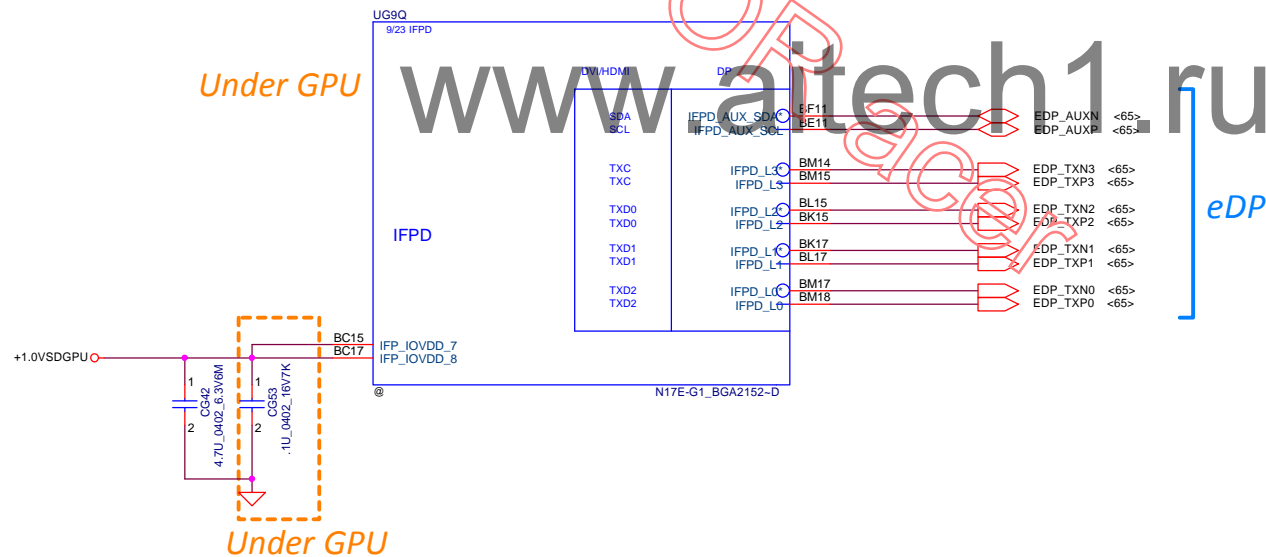
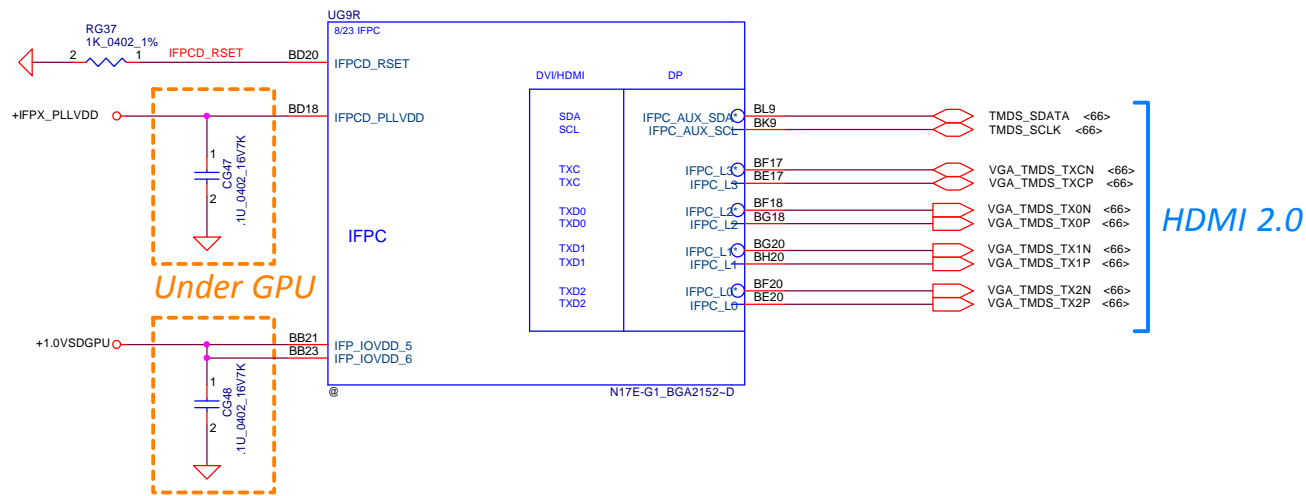
	22uF	10uF	4.7uF	1uF	0.1uF
IFPx_IOVDD			3	1	6
IFPx_PLLVDD	1				2

		PH	PD		
I2CS_SCL	VGA_SMB_CK2	1.8K		to EC, provide internal thermal sensor information	
I2CS_SDA	VGA_SMB_DA2	1.8K			
I2CC_SCL	I2CC_SCL_R	1.8K		to GPU_B+ sensor (INA3221)	
I2CC_SDA	I2CC_SDA_R	1.8K			
I2CB_SCL		1.8K		reserved NVIDIA use only	
I2CB_SDA		1.8K			
GPI00	NVVDD_VID			PWM Output to control NVVDD (NVVDD1)	
GPI01	DGPU_GC6_FB_EN		10K	FB EN for GC6 2.1	
GPI02	GPU_EVENT#_D	10K		GPU wake signal for GC6 2.1	0.D.
GPI03	NVVDDS_VID			PWM output to control the SRAM power supply (NVVDD2)	
GPI04	I1V8_MAIN_EN	10K		GPU power sequencing for GC6 2.1	0.D.
GPI05	FRAME_LOCK#	10K		Active low, for G-synce	0.D.
GPI06	NVVDD_PSI	10K		to disable some phases of core power supply	
GPI07	GPU_INV_PWM		100K	for eDP INV_PWM	
GPI08	MEM_VDD_CTL			for memory voltage control (1.35V to 1.55V)	0.D.
GPI09	ALERT	10K		use internal thermal sensor, this pin Only PU	0.D.
GPI010	MEM_VREF		100K	NV require control over this pin when lowering MEM p-state	
GPI011	DGPU_ENVDD		100K	EN LCD_VDD	
GPI012	DGPU_AC_DETECT	100K		monitoring AC to DC action and divide core freq. by 4	
GPI013	GPU_ENBKL		100K	tell EC to EN panel back light	
GPI014	DPO_HPD_GPU#	10K		HPD for Type-C DP	
GPI016	SYS_PEX_RST_MON#	10K		because self drive rest, only need to PU	
GPI017	DGPU_EDP_HPD#	10K		HPD for eDP	
GPI018	DGPU_DP4_HPD#	10K		HPD for DP4	
GPI020	NVVDDS_PSI	10K		For NVVDD2 PWR saving	
GPI021	Master_SLI_RASTER_SYNC0		100K	Input for Master/ Output from Slave	0.D.
GPI022	Master_SLI_SWAPRDY_IN	1K		an active-low open-drain connection between Master and Slave GPU	0.D.
GPI023	GPU_PEX_RST_HOLD#	10K		because self drive rest, only need to PU	0.D.
GPI024	DGPU_DP5_HPD#	10K		HPD for DP5	
GPI027	DGPU_HDMI_HPD#			HPD for HDMI	
GPI028	OC_WARN#	10K		Over Current Throttling trigger.	
OVERT	OVERT	10K		to Thermal shut down logic	0.D.

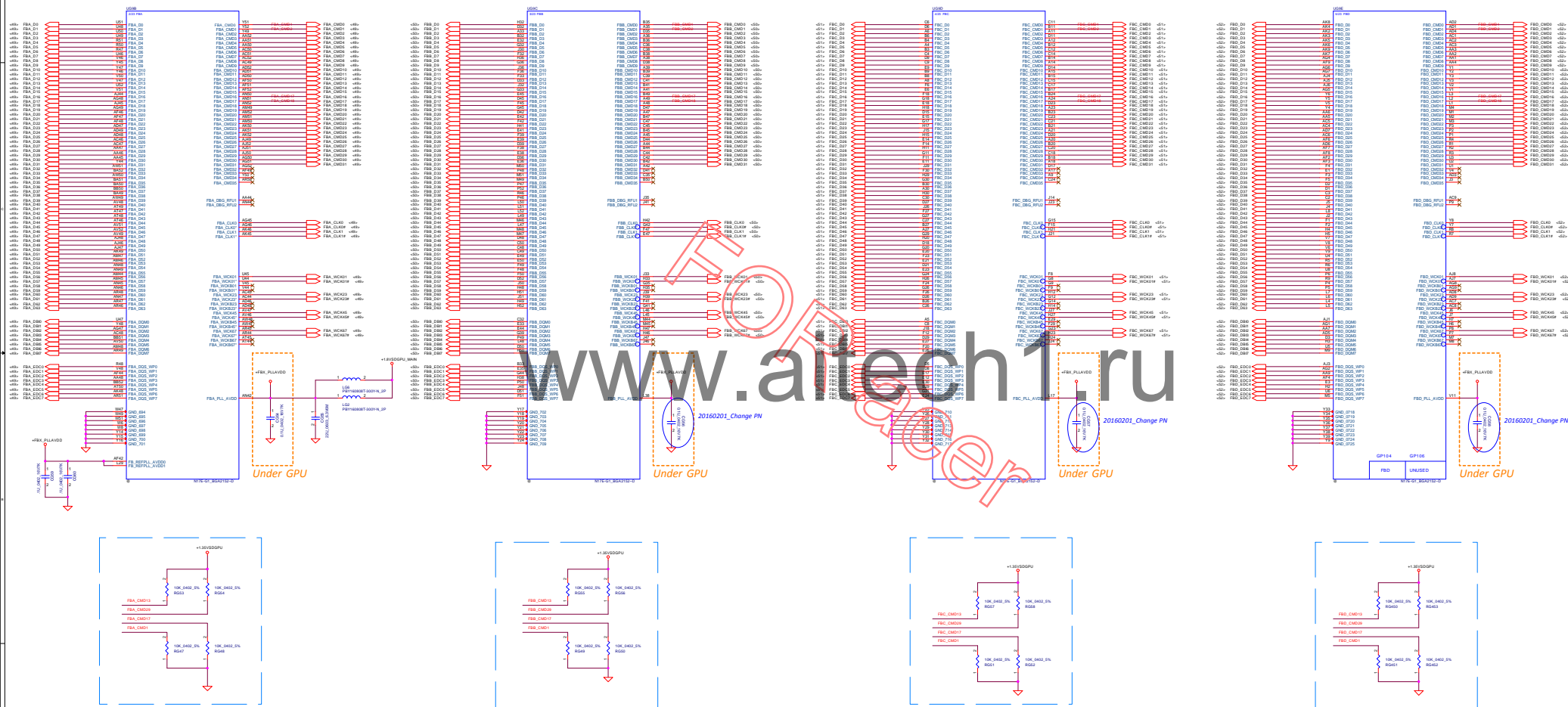


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				C1PR2 LA-E051P		1.0
				Date:	Monday, January 09, 2017	Sheet 42 of 103





Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2016/02/01	Deciphered Date	2017/12/31	Title	N17E-G1(1/6) PCIE,GPIO
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				Date	Monday, January 09, 2017
				Sheet	43 of 103
				Rev	1.0
				CIPR2 LA-E051P	





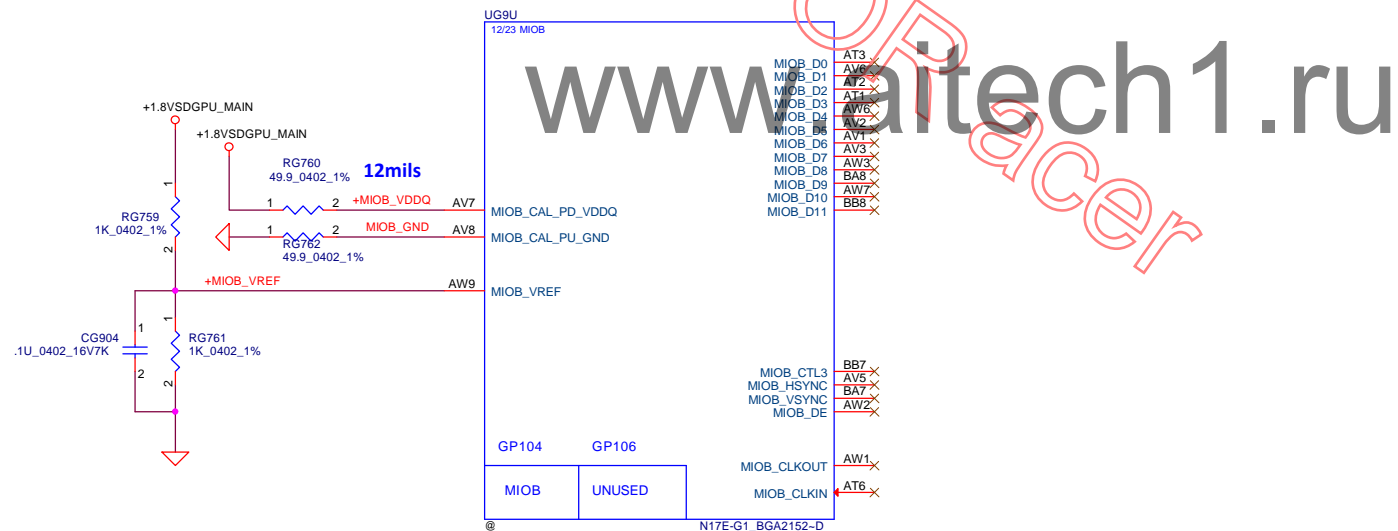
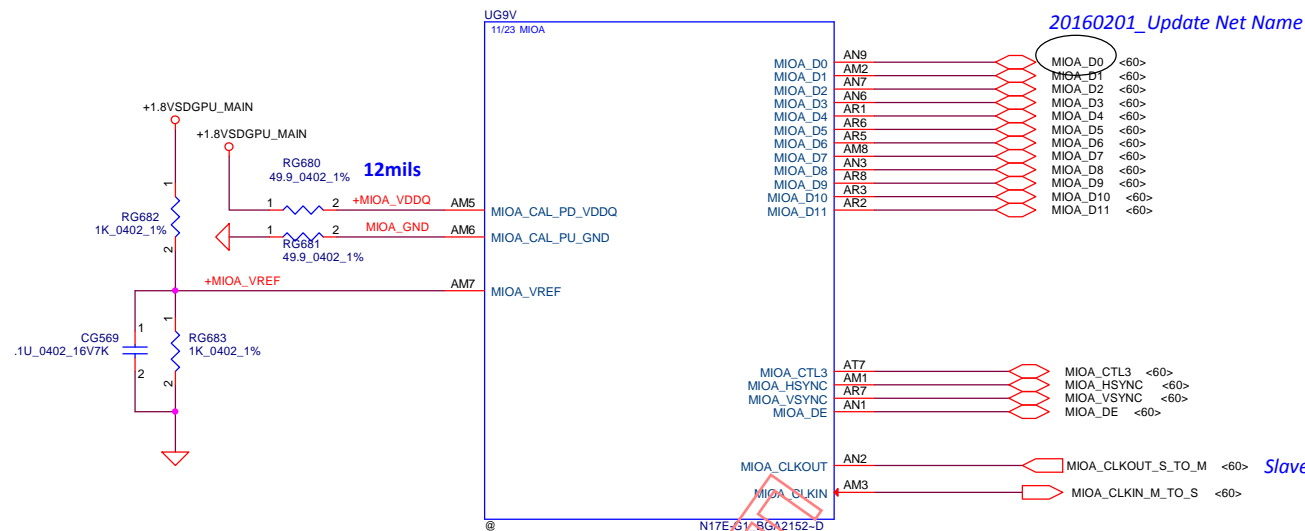


**X**

**X**

**X**

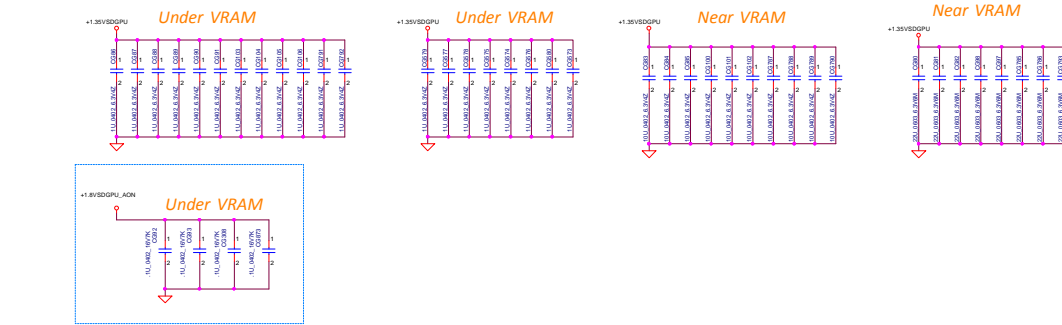
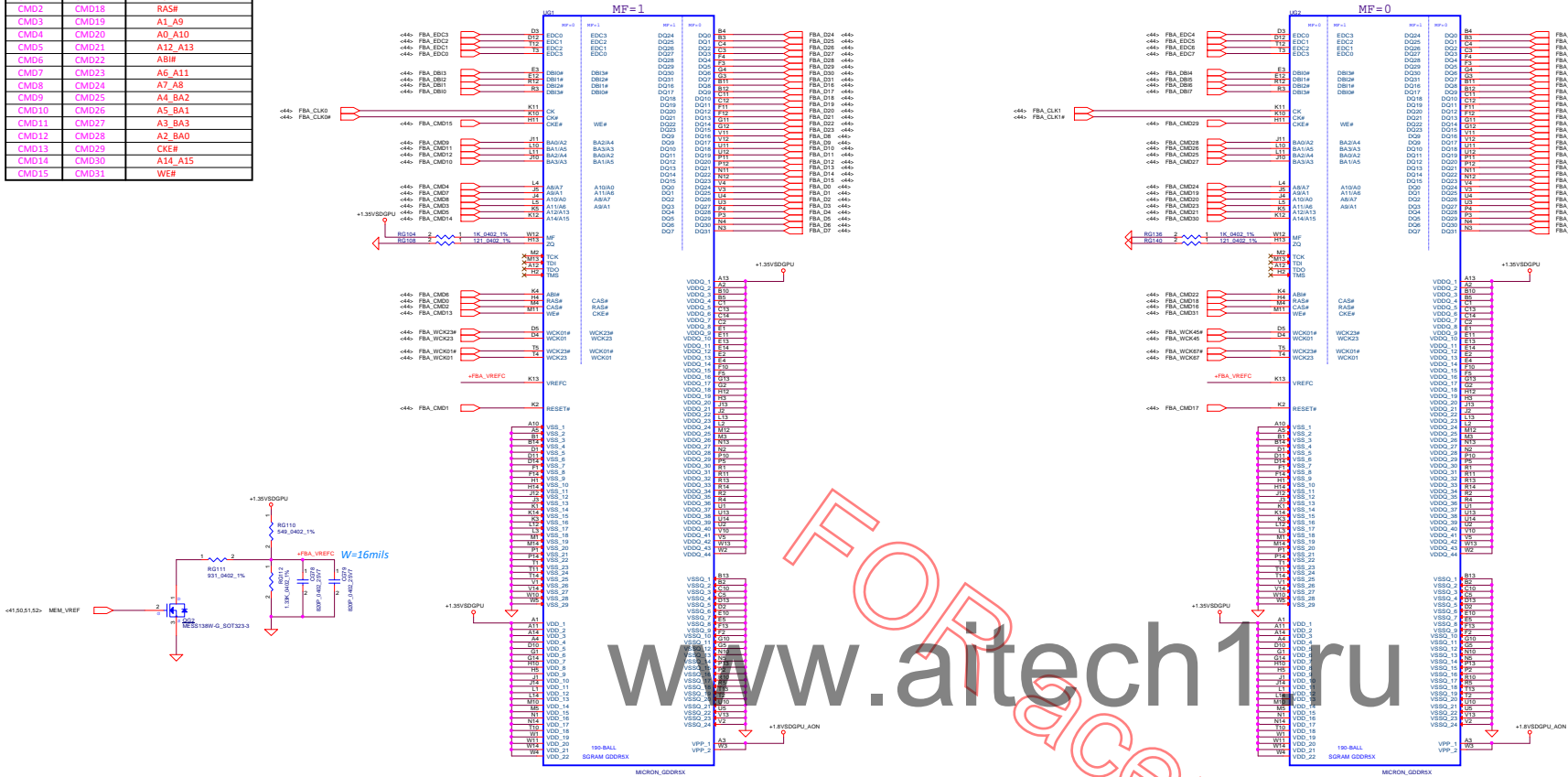




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				Date:	Monday, January 09, 2017
				Sheet	48 of 103
				Rev	1.0
				Sheet	48 of 103

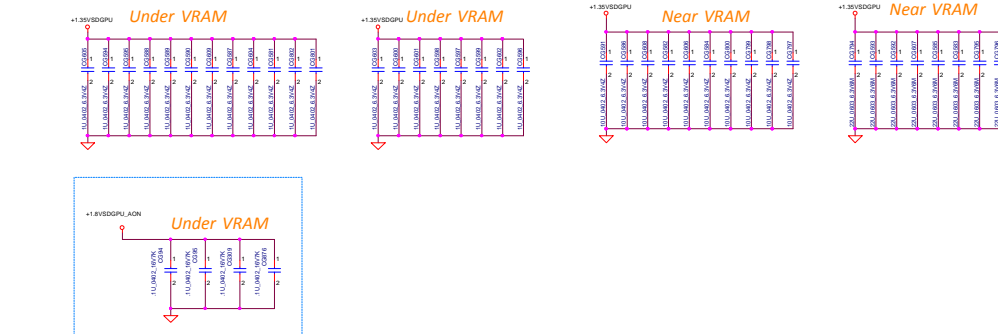
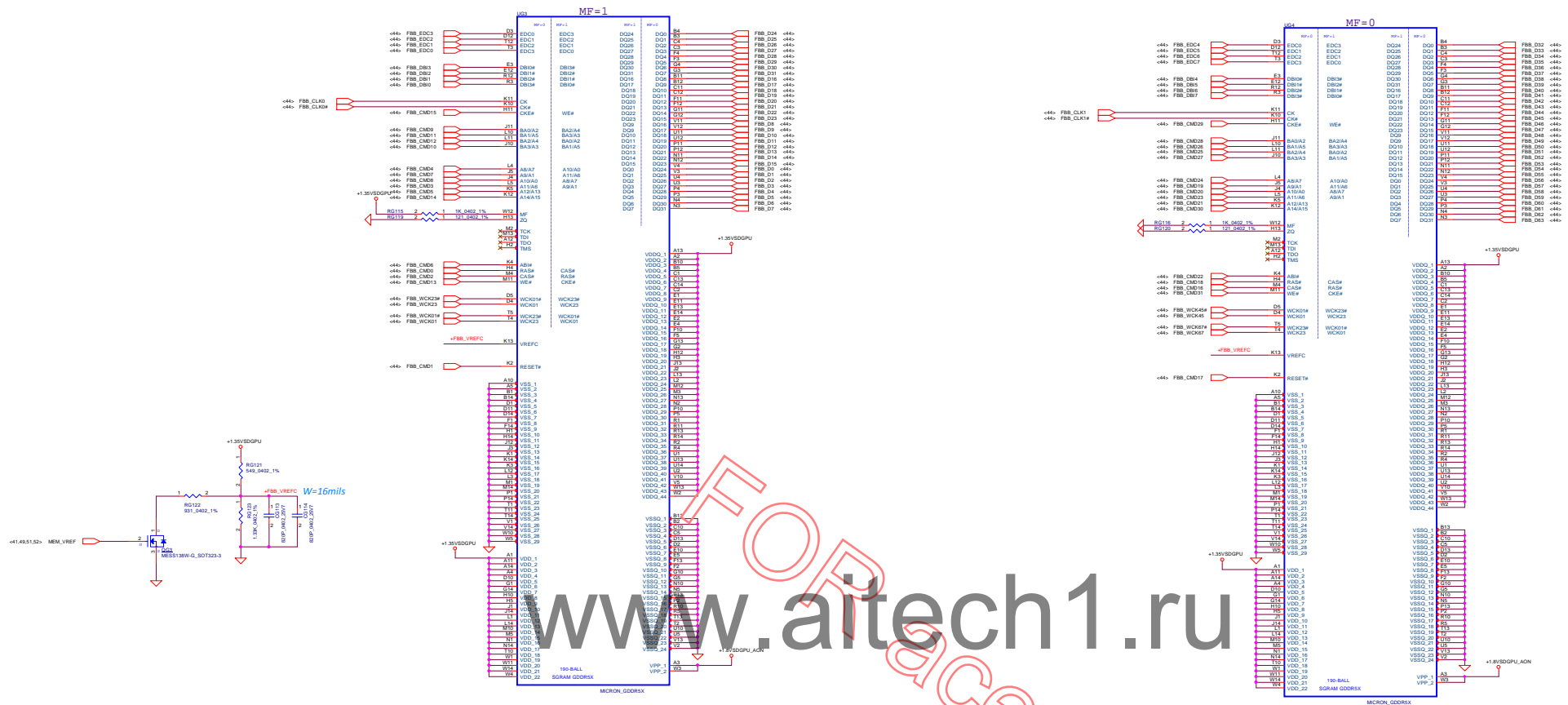


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CM01	CM017	RST#
CM02	CM018	RAS#
CM03	CM019	A1_A9
CM04	CM020	A0_A10
CM05	CM021	A12_A13
CM06	CM022	AB#
CM07	CM023	A6_A11
CM08	CM024	A7_A8
CM09	CM025	A4_BA2
CM10	CM026	A5_BA1
CM11	CM027	A3_BA3
CM12	CM028	A2_BA0
CM13	CM029	CKE#
CM14	CM030	A14_A15
CM15	CM031	WE#



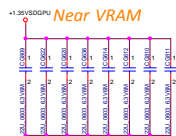
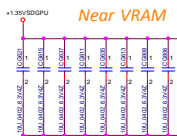
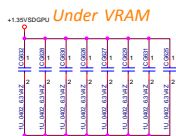
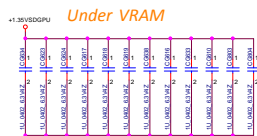
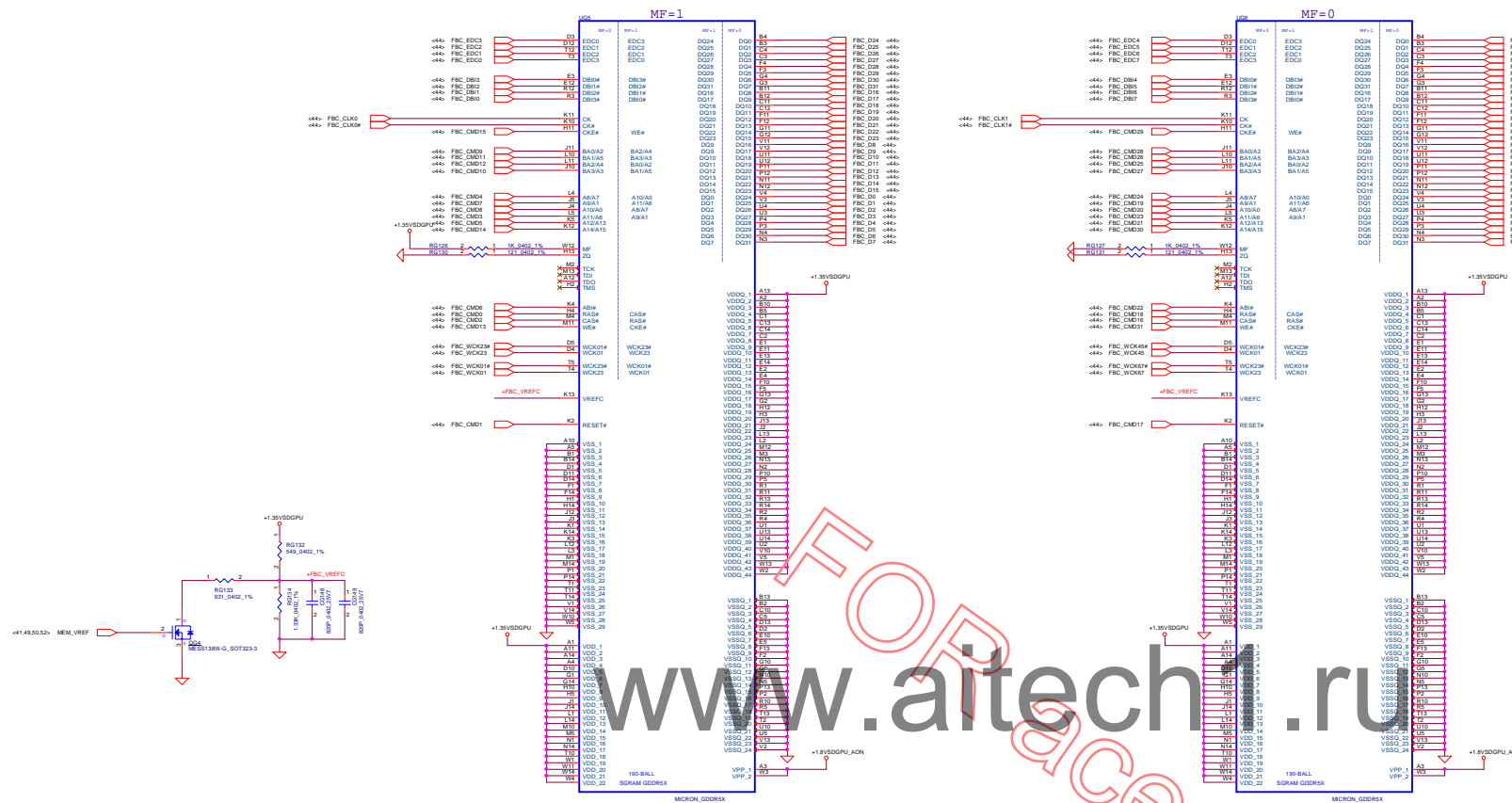
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VDD	4	5		12	
VDDQ	4	5		8	

Security Classification	2016/03/01	Compul Secret Data	2017/12/31	Yes	Compul Electronics, Inc.
Issued Date	2016/03/01	Discontinued Date	2017/12/31	Yes	N17E-GDDR5 A-M
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Part	CIPR2 LA-E051P	Rev	1.0	100	100

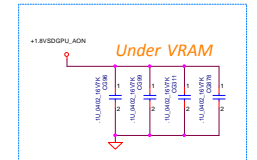


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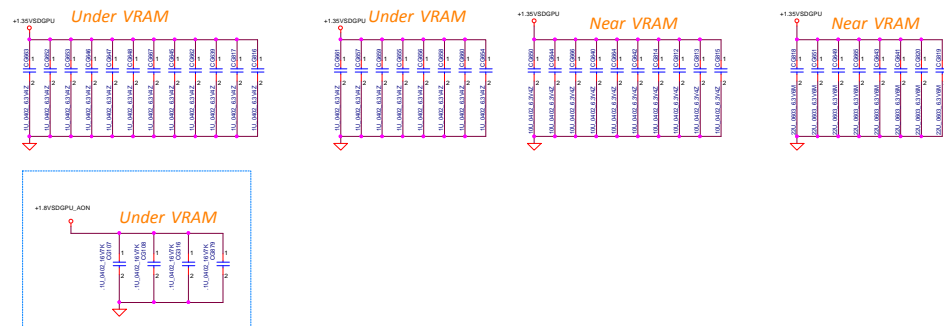
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				CIPR2 LA-E051P	
				Rev 1.0	



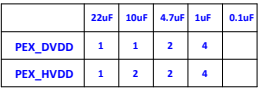
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VDD	4	5		12	
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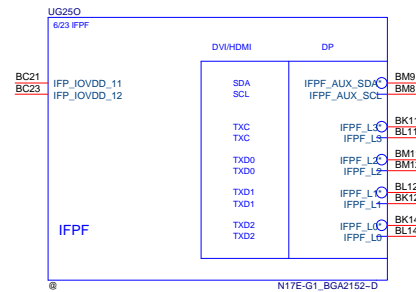
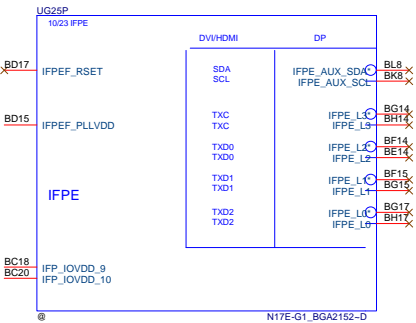
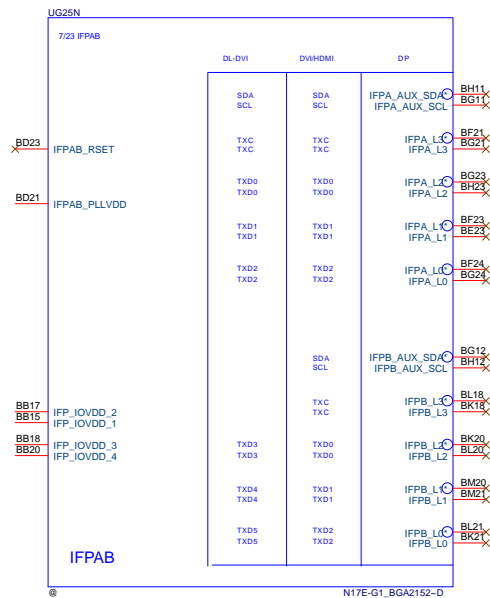


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Issued Date	2016/03/01	Discontinued Date	2017/12/31	Yes
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NITE-GDDR5 C-M				
CIPR2 LA-E051P				
Date: March, January 18, 2017				Sheet 51 of 103



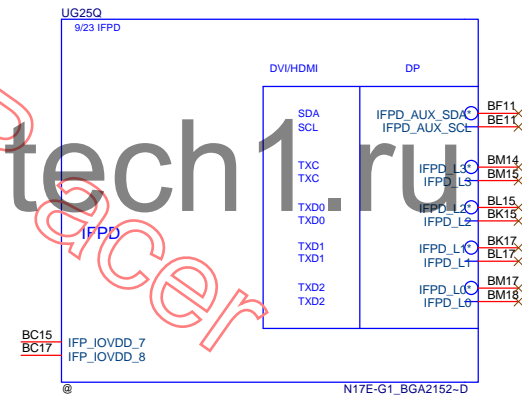
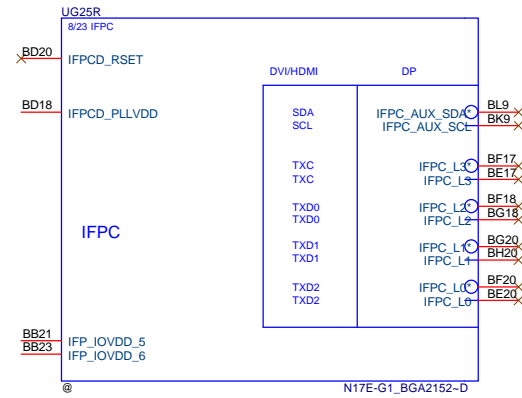
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VDD	4	5		12	
VDDQ	4	5		8	





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IFPx_PLLVDD	1				2

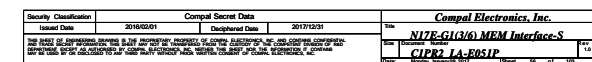




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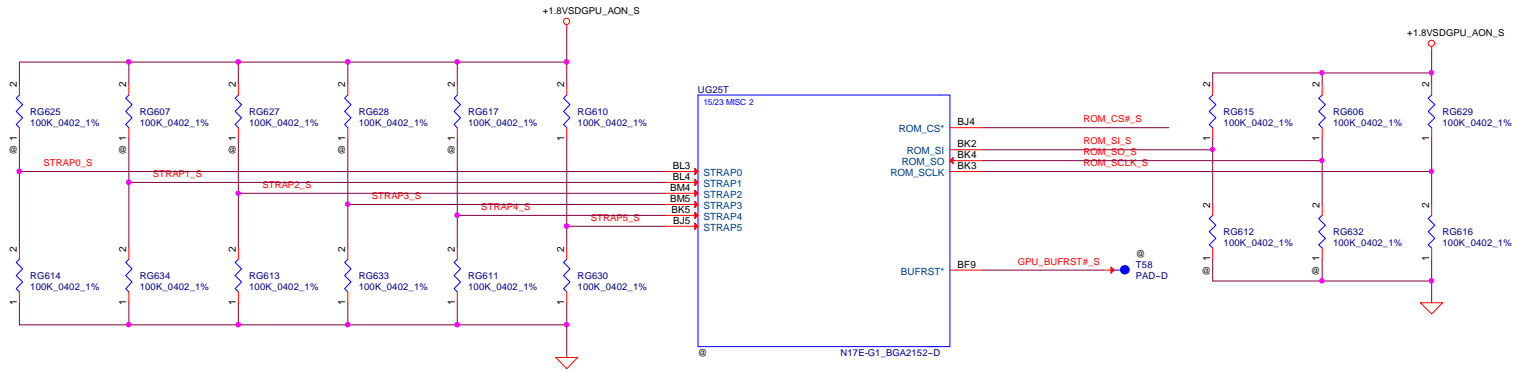
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Issued Date	2016/02/01	Deciphered Date	2017/12/31	Title	
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				Rev	
				1.0	
				Date:	Monday, January 09, 2017
				Sheet	55 of 103





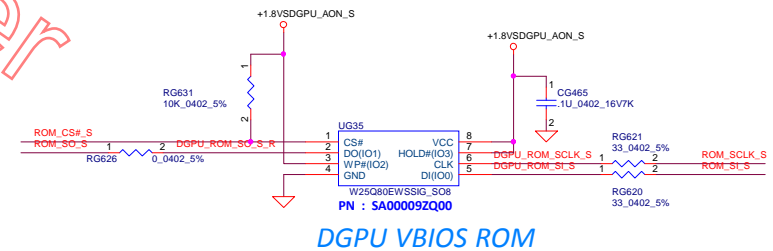
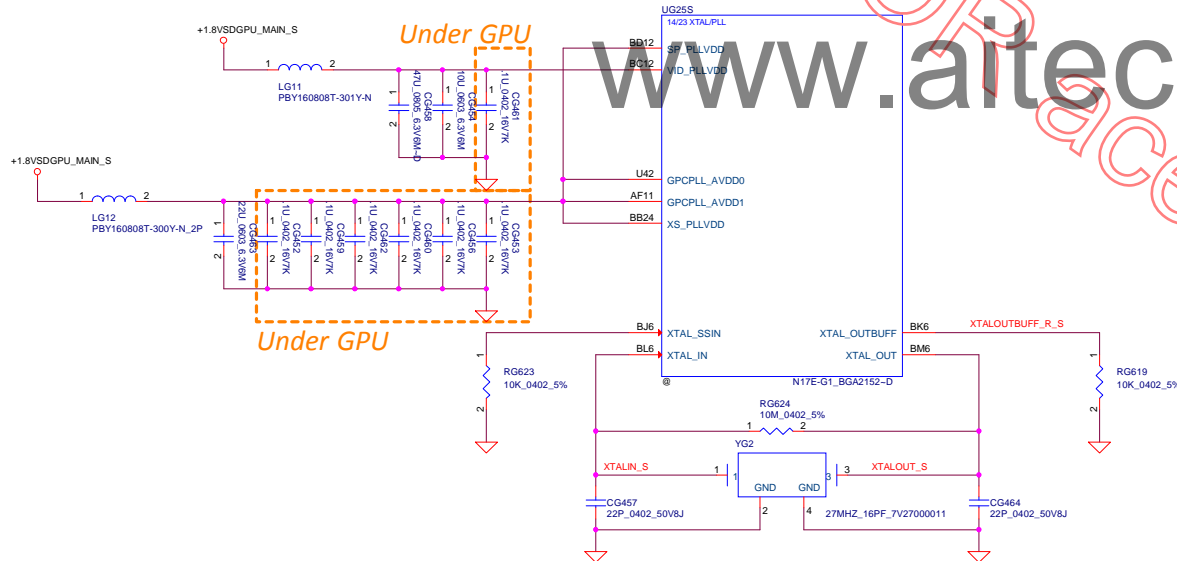


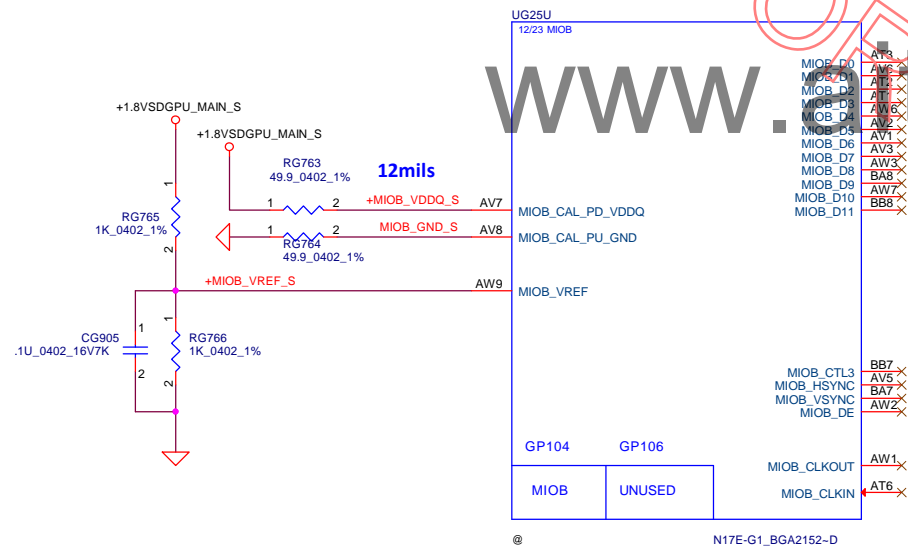
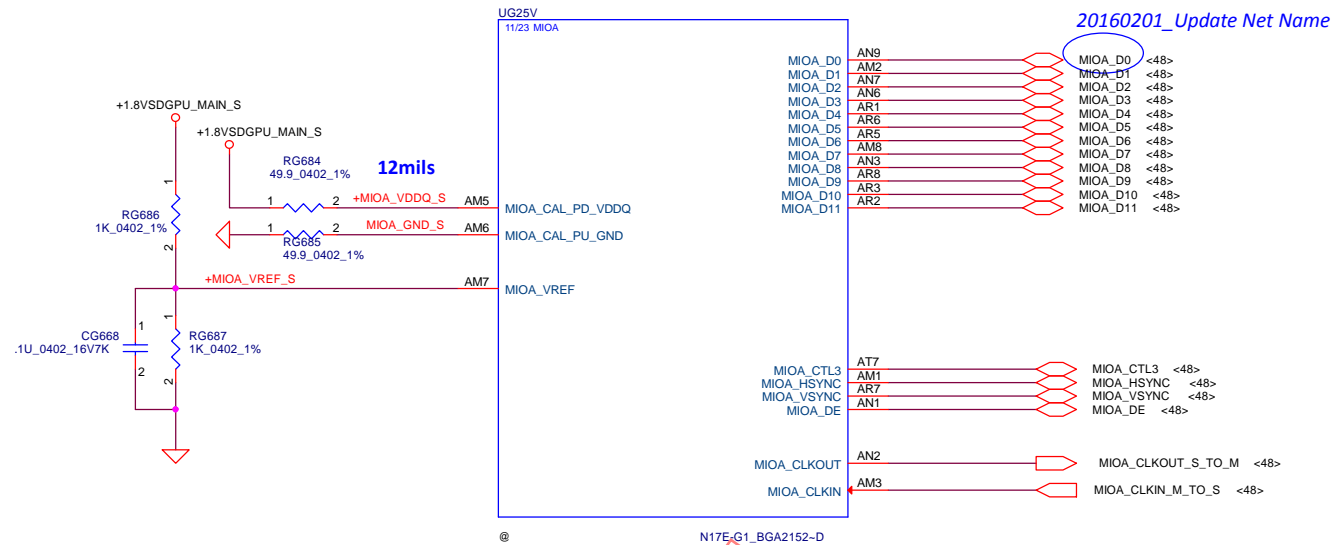
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VID_PLLVDD	1		1			1
SP_PLLVDD GPCPLL_AVDD		1				6



**MICRON  
MT58K256M32 - 100:A**

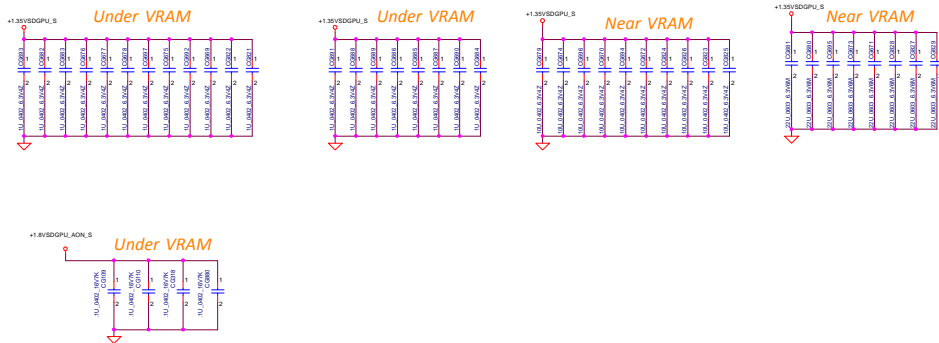
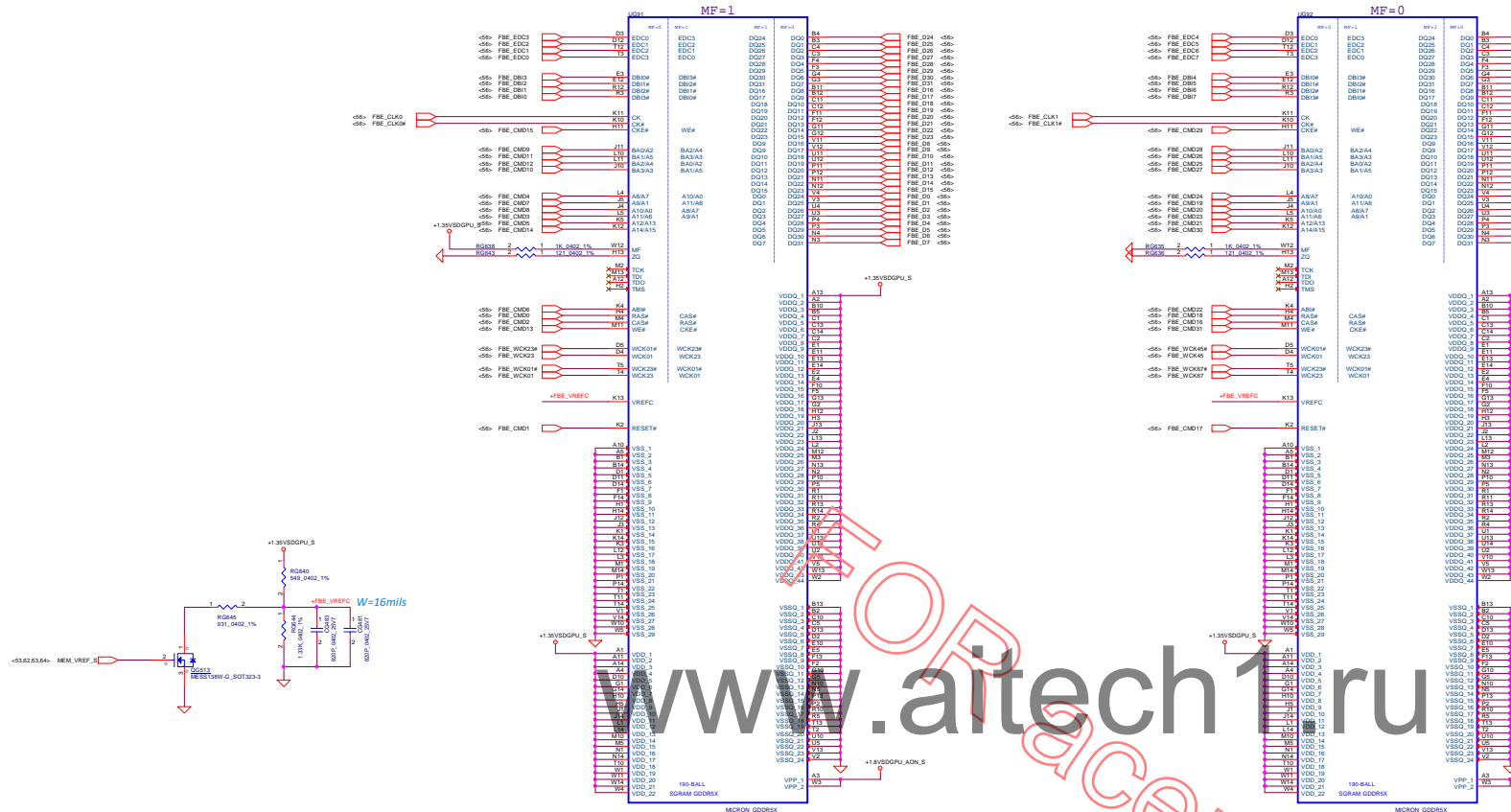
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Master	PD 100kOhm	PD 100kOhm	PD 100kOhm	PU 100kOhm	PD 100kOhm	PU 100kOhm	PD 100kOhm	PD 100kOhm	PD 100kOhm
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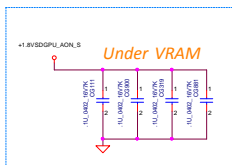
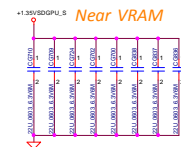
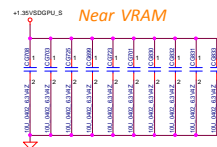
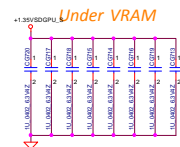
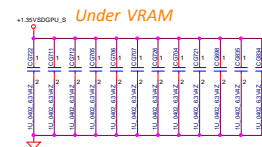
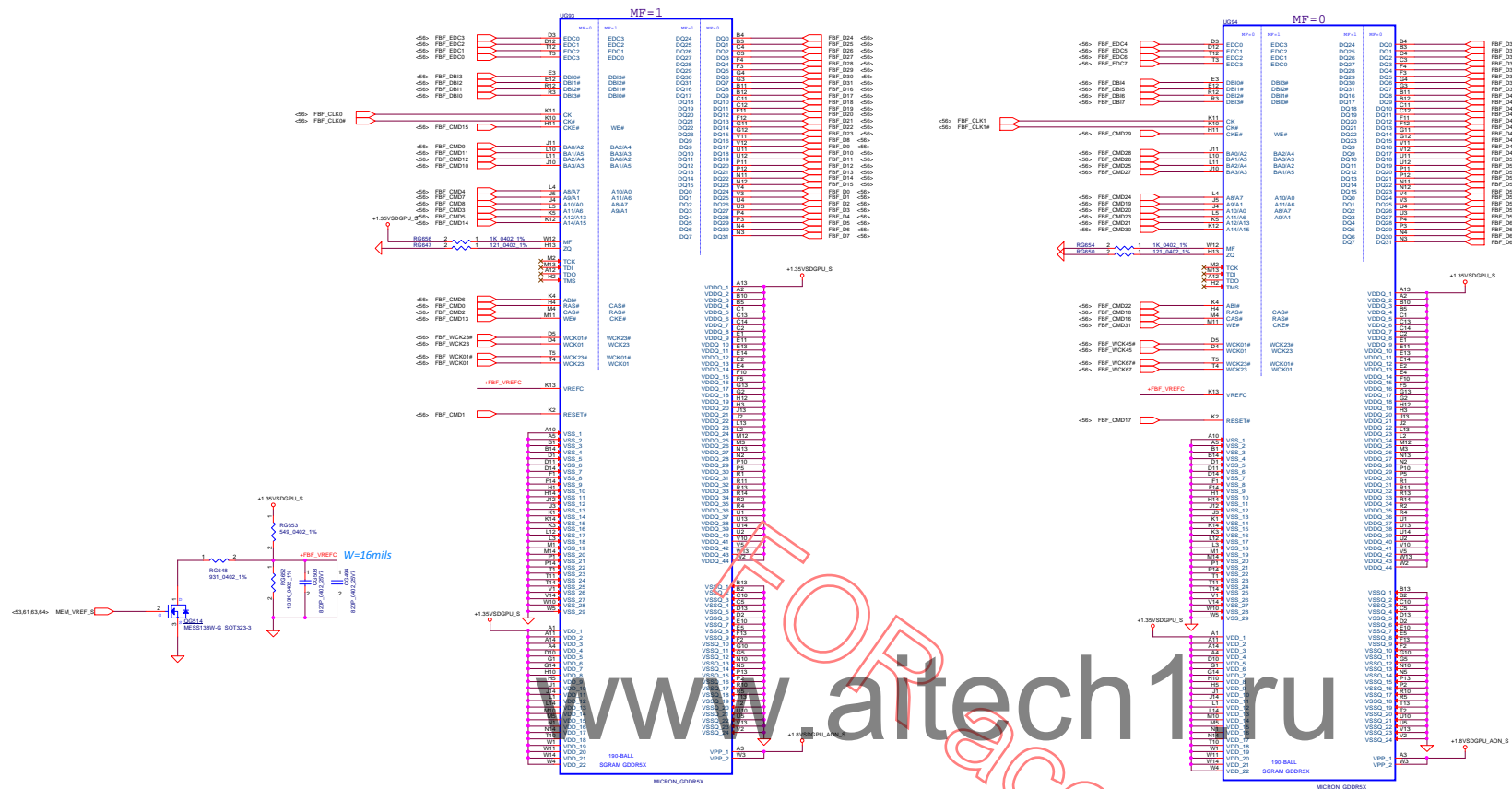
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Issued Date	2016/02/01	Deciphered Date	2017/12/31	Title	N17E-G1(1/6) PCIE,GPIO
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				Date:	Monday, January 09, 2017
				Sheet	60 of 103
				Rev	1.0
				CIPR2 1A-E051P	





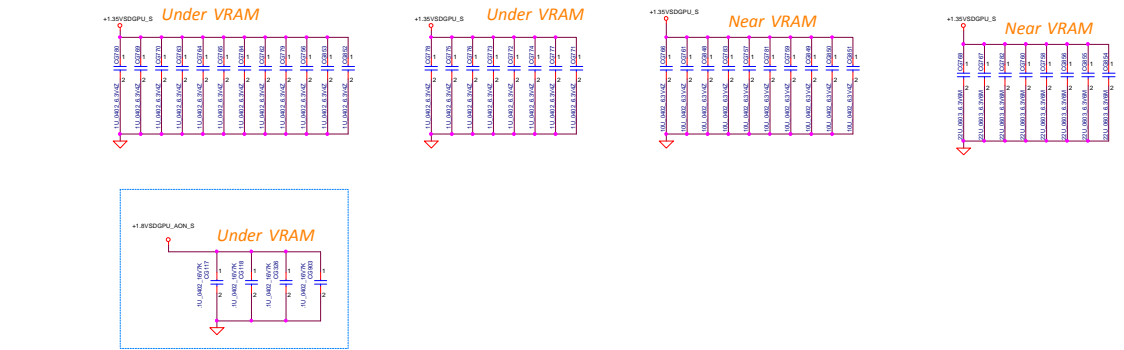
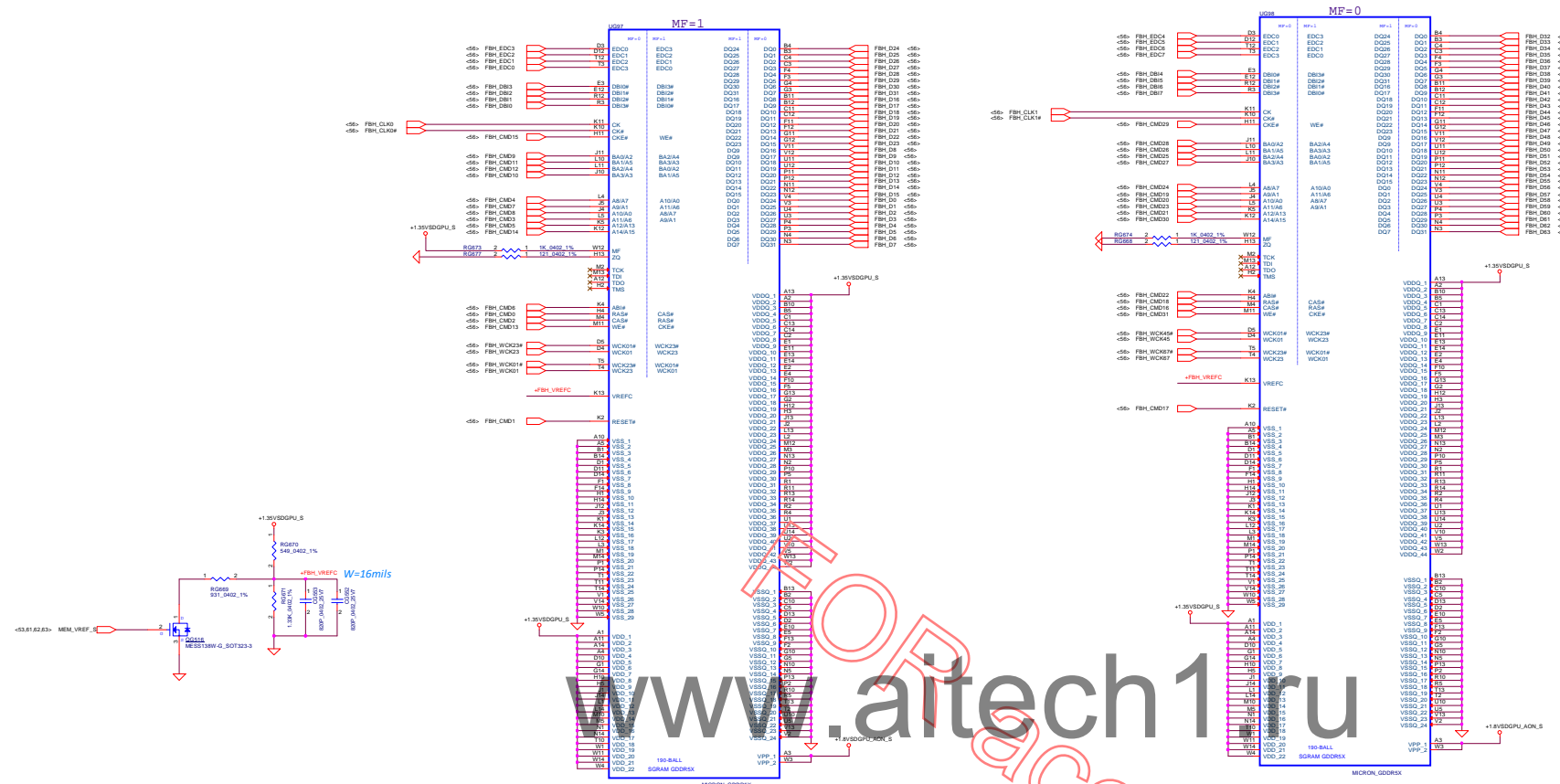
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VDD	4	5		12	
VDDQ	4	5		8	

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				Rev	1.0
				10sheet 61 of 103	



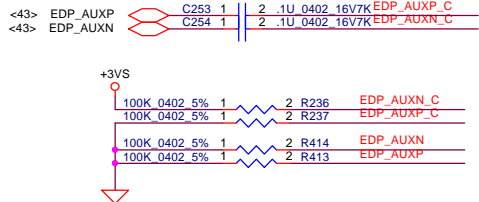
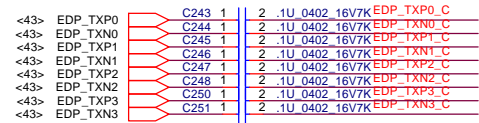
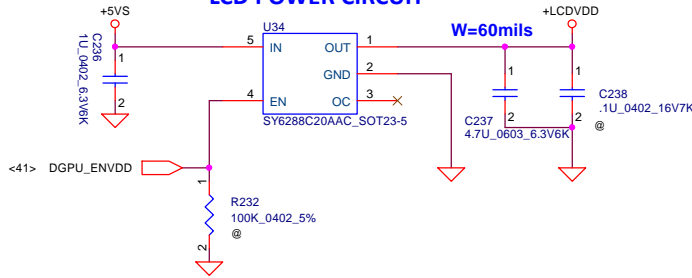
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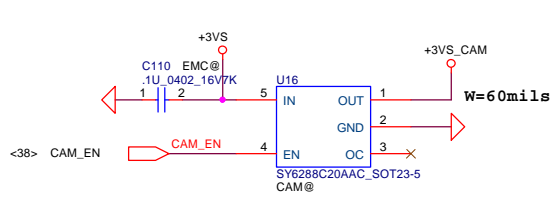


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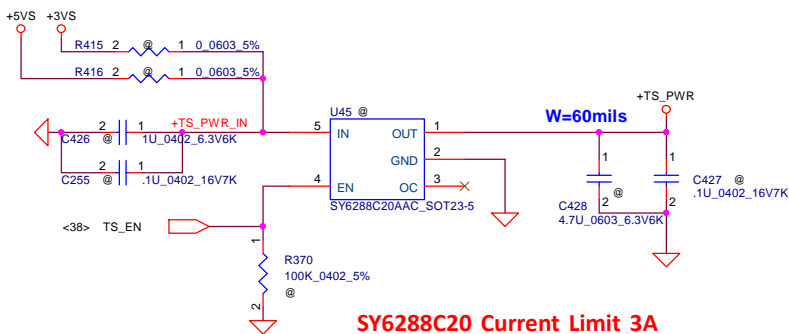
## LCD POWER CIRCUIT



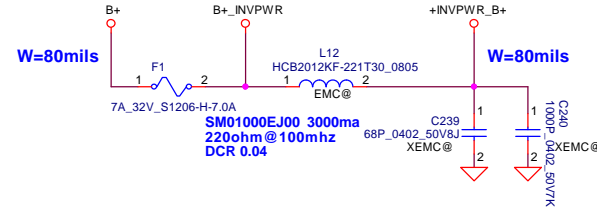
## HD CAM POWER CIRCUIT



## TS POWER CIRCUIT

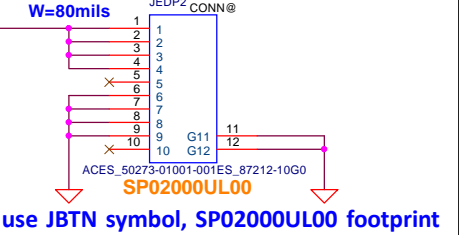


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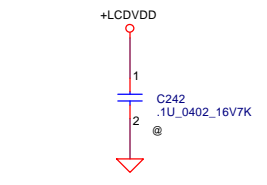


## LED PANEL Conn.

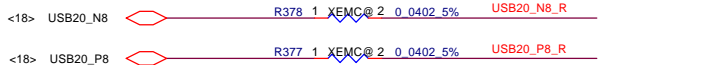
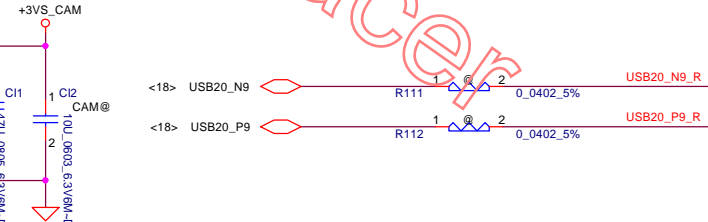
W=80mils



Place closed to JEDP1



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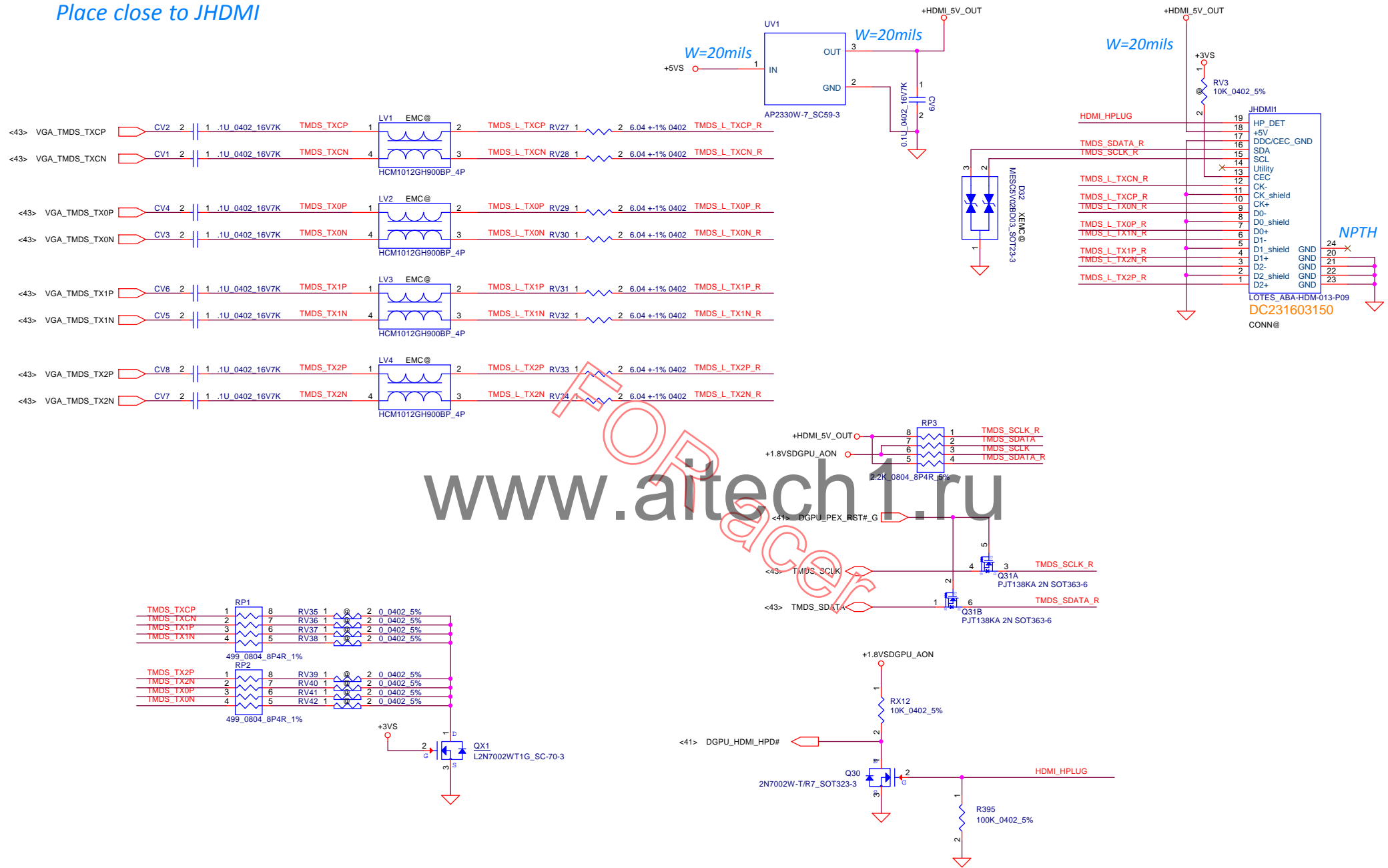
Touch Screen

HD Cam

default floating

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Size				Document Number				Rev			
Custom				Monday, January 09, 2017				Sheet 65 of 103			
Date				Monday, January 09, 2017				Sheet 65 of 103			

Place close to JHDMI

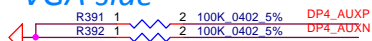


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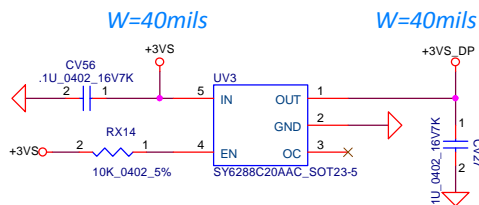
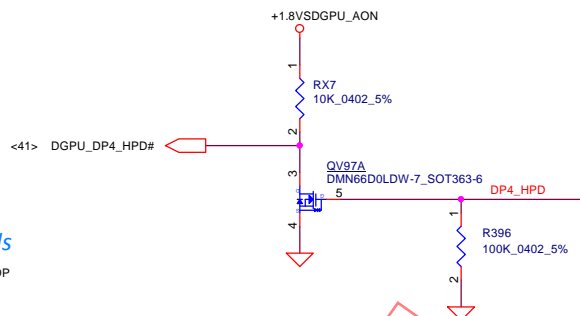
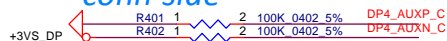
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Issued Date	2016/02/01	Deciphered Date	2017/12/31	Title	
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Size	Document Number	CIPR2 LA-E051P		Rev	1.0
Date:	Monday, January 09, 2017	Sheet	66 of 103		



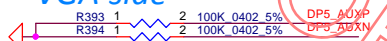
# VGA side



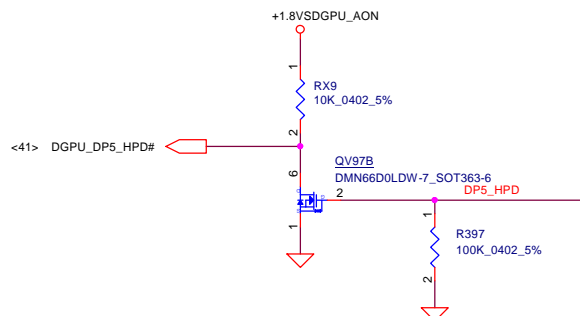
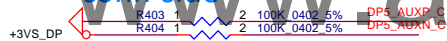
# conn side



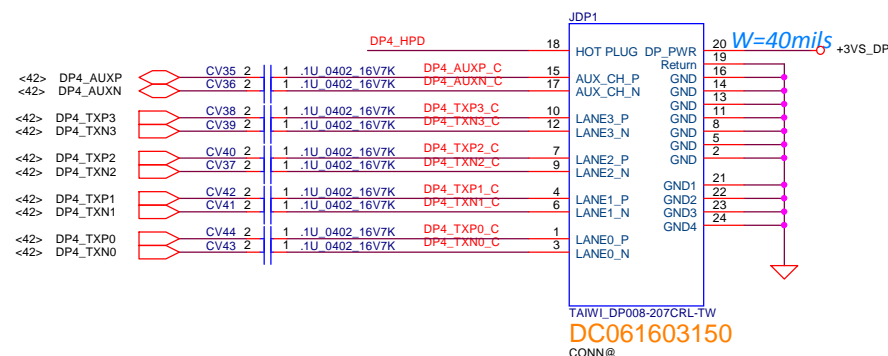
# VGA side



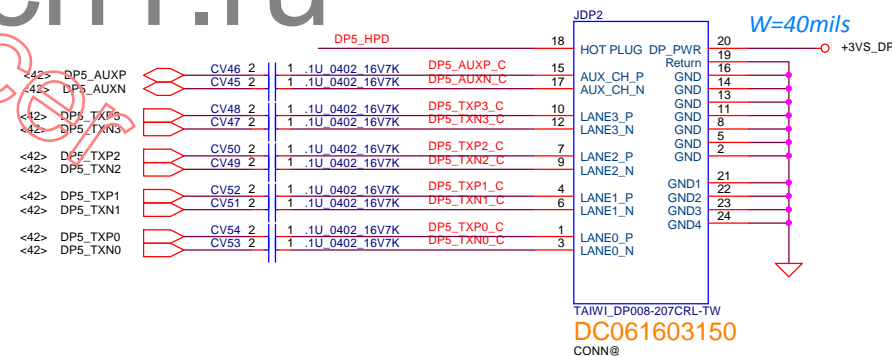
# conn side



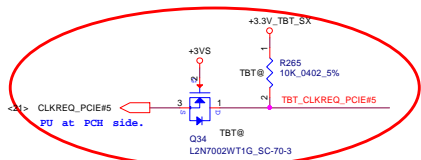
# Display Port



# Display Port



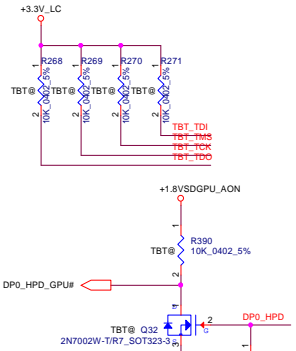
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Issued Date	2016/02/01	Deciphered Date	2017/12/31	Title	
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Size	Document Number	Rev		1.0	
Custom	CIPR2 LA-E051P	Date:		Monday, January 09, 2017	
Sheet		67		of 103	



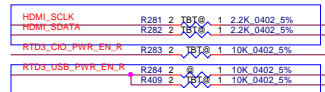
PCIE\_X4\_Bus  
(Link to PCH Port 5-8)

PCIE\_CLK  
(From PCH CLKOUT0)

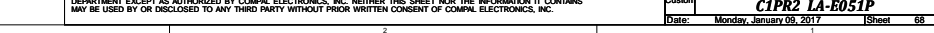
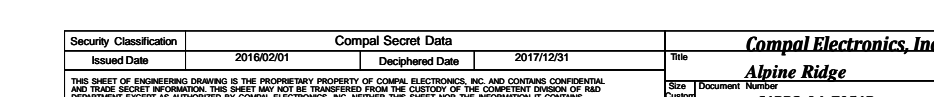
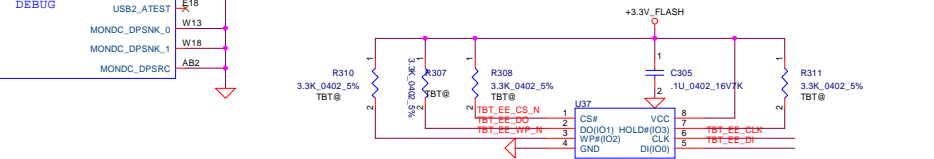
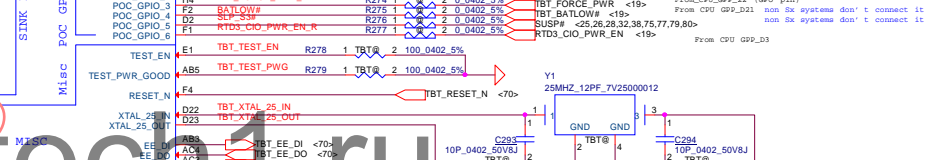
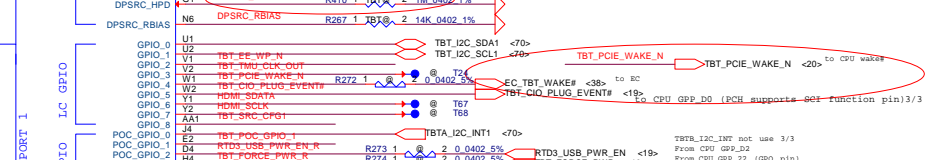
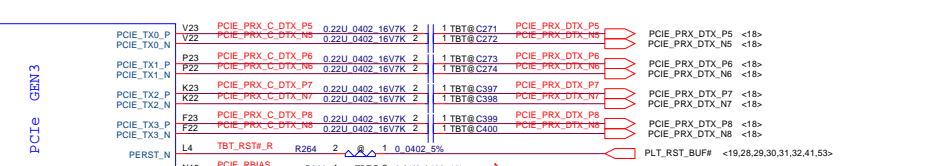
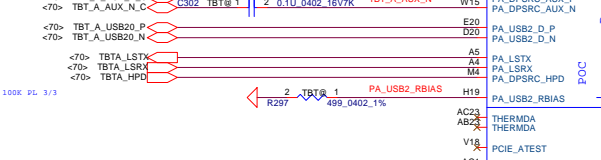
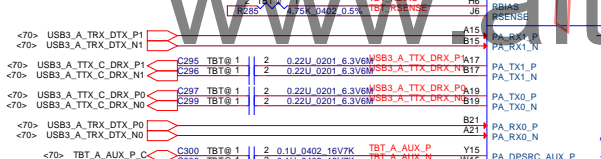
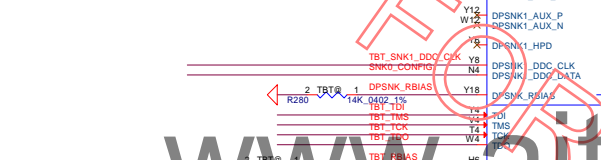
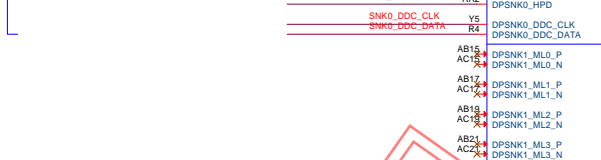
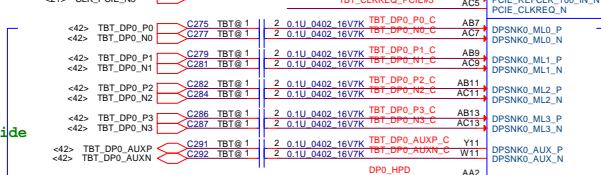
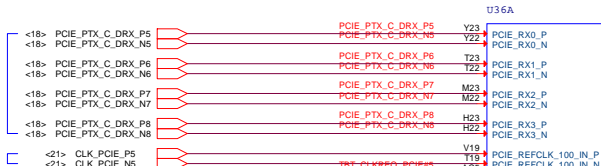
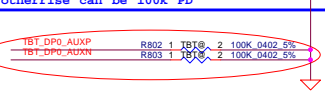
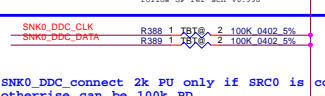
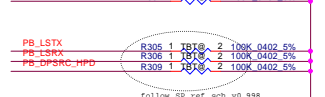
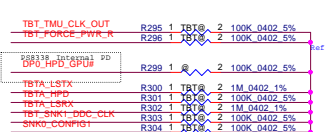
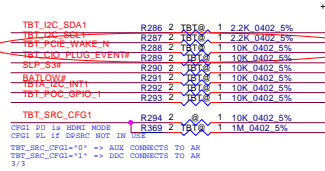
DDC:3.3V  
PU @ SOC side



Follow Intel recommend, 5/4.



Follow Intel recommend, 4/28.



POC_GPIO_0	interrupt from port power switch
POC_GPIO_1	interrupt from port power switch
POC_GPIO_2	rtdd3 power enable for USB mode
POC_GPIO_3	force full power on
POC_GPIO_4	bat try low indication
POC_GPIO_5	slp_s3 system indication
POC_GPIO_6	rtdd3 power enable for cio mode

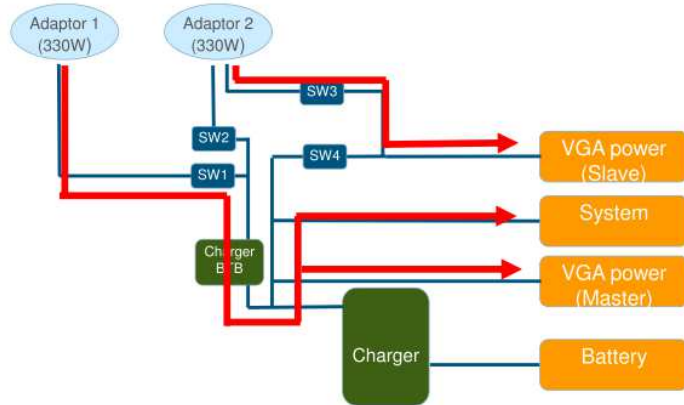
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Issued Date	2016/02/01	Deciphered Date	2017/12/31	Alpine Ridge
Document Number	C1PR2 LA-E051P			
Date	Monday, January 09, 2017	Sheet	68	of 103

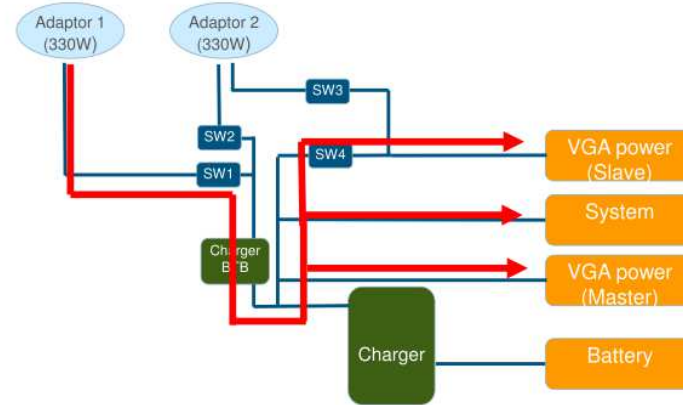




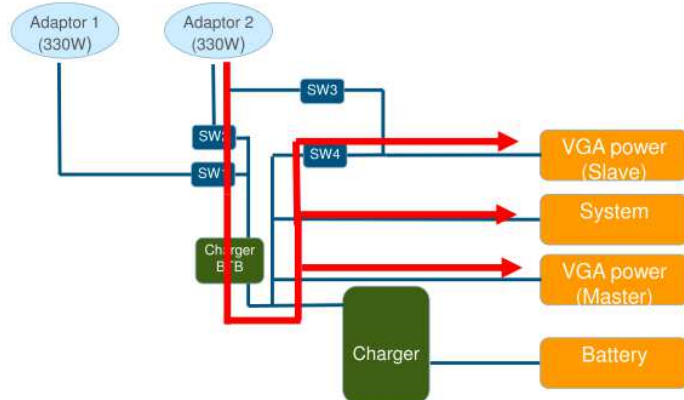
Adaptor1 + Adaptor 2



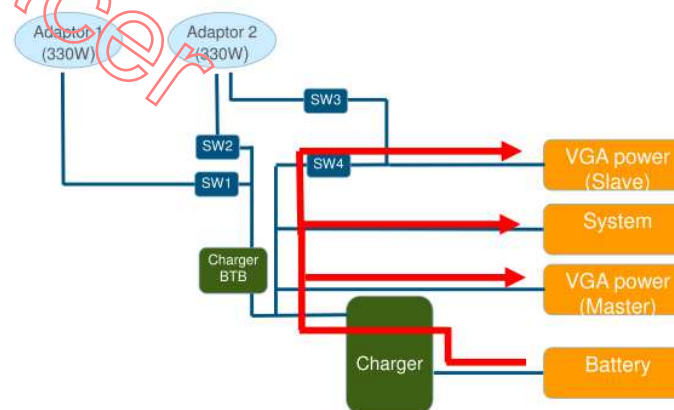
Adaptor1 only



Adaptor2 only

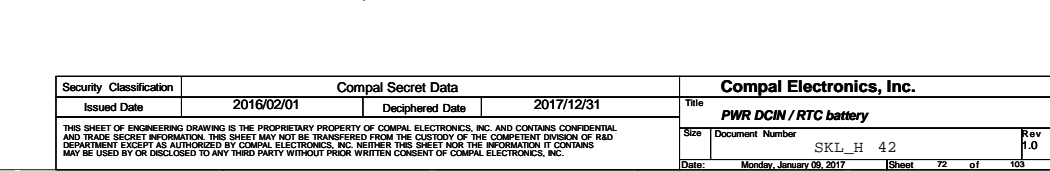
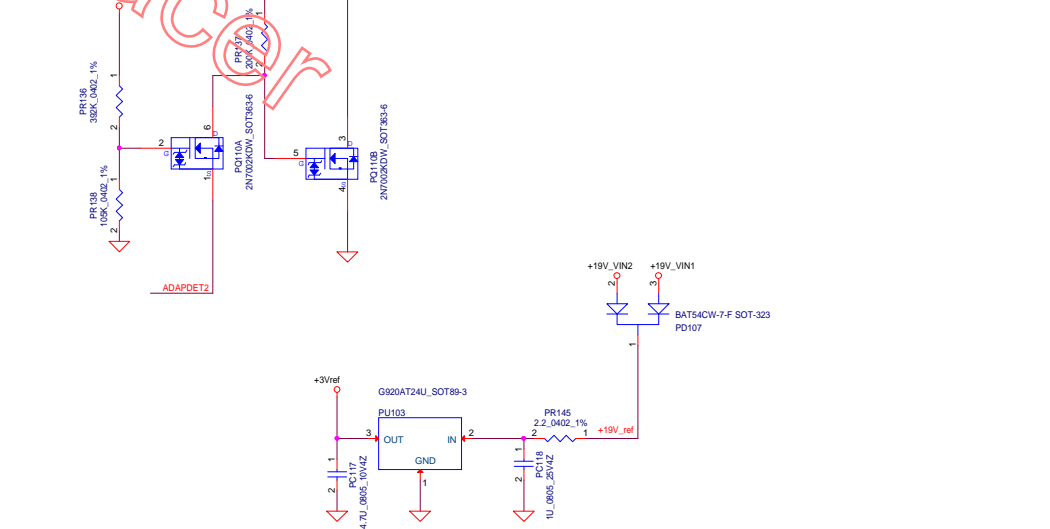
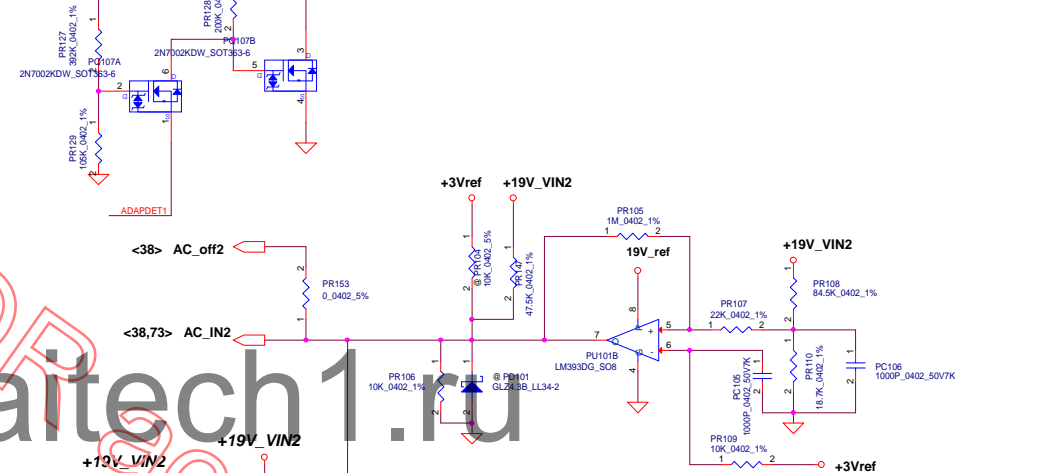
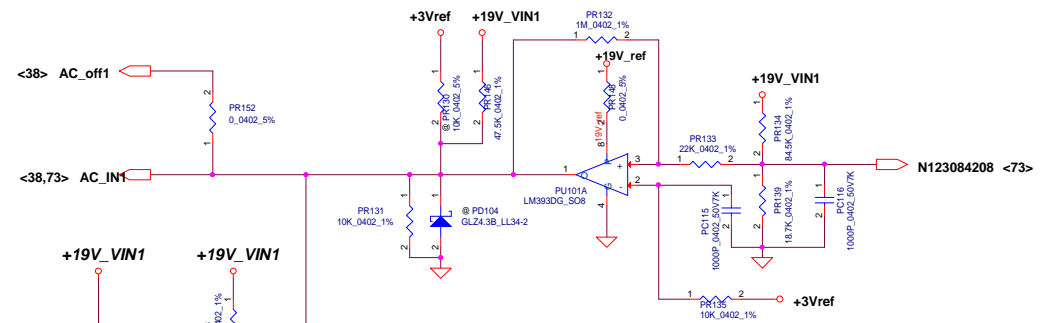
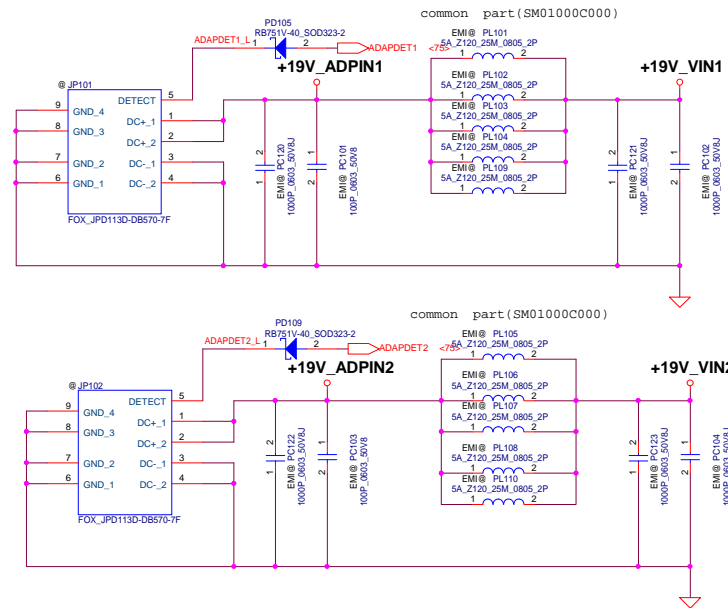


DC mode



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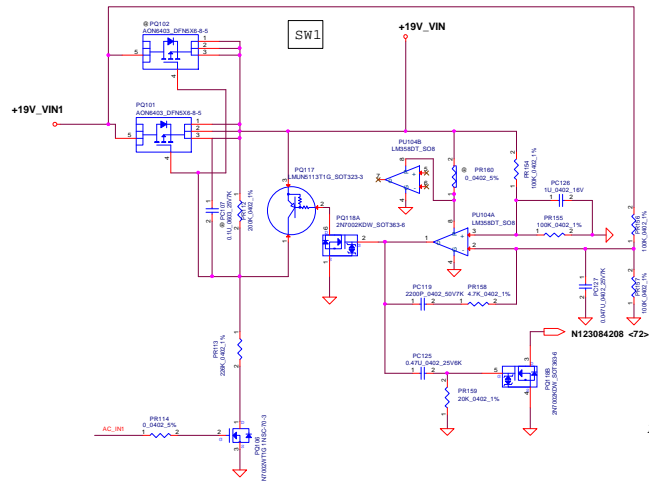
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				Size	Document Number
				Custom	C1PR2 LA-E051P
				Date	Monday, January 09, 2017
				Sheet	71 of 103
				Rev	1.0



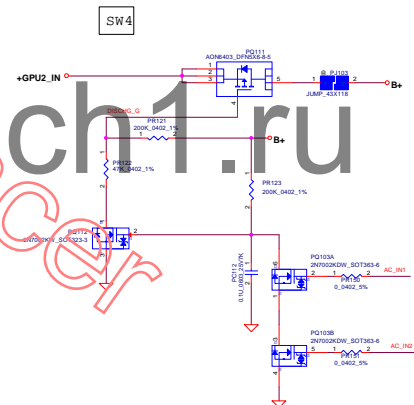
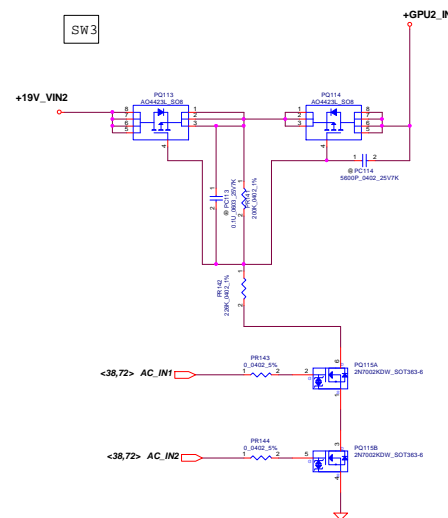
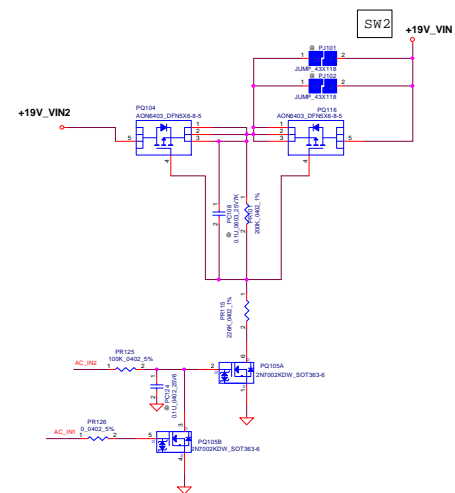
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Size	Document Number	SKL_H 42	Rev	1.0
Date:	Monday, January 09, 2017	ISheet	72	of 103

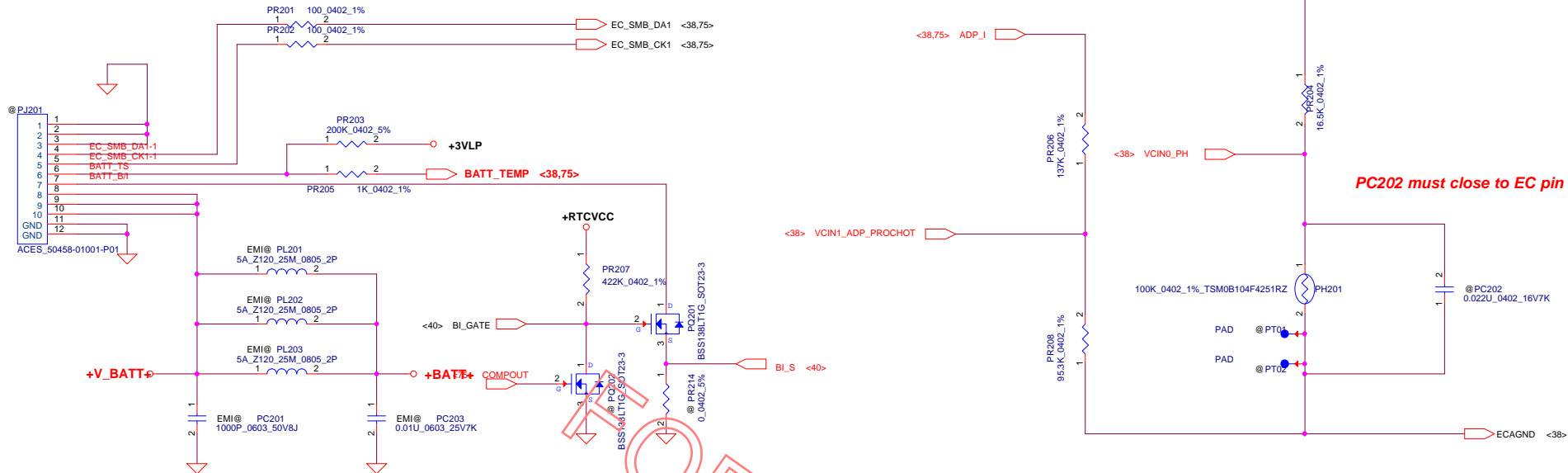




	ACIN1=1	ACIN1=0
ACIN2=1	SW1→ ON SW2→ OFF SW3→ ON SW4→ OFF	SW1→ OFF SW2→ ON SW3→ OFF SW4→ ON
ACIN2=0	SW1→ ON SW2→ OFF SW3→ OFF SW4→ ON	SW1→ OFF SW2→ OFF SW3→ OFF SW4→ ON



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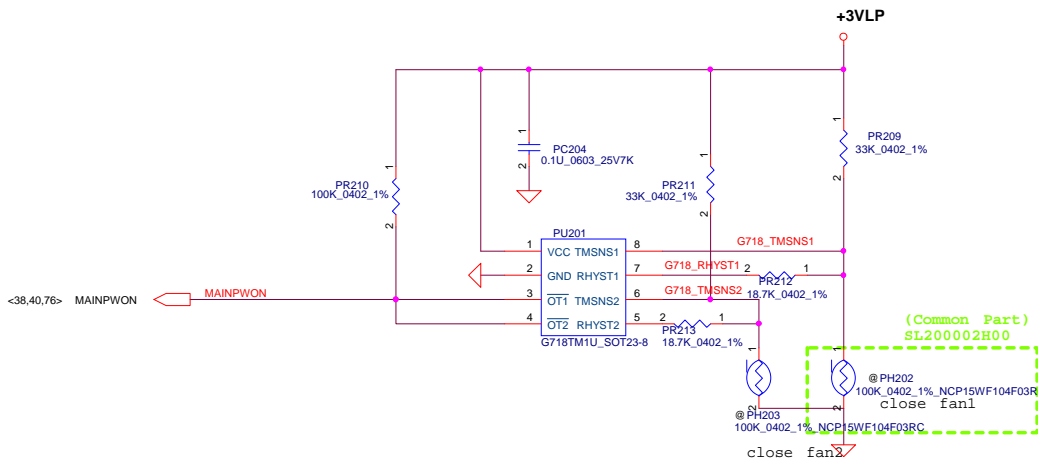


---Battery\_pin define---

PIN1 GND  
PIN2 GND  
PIN3 GND  
PIN4 SMD  
PIN5 SMC  
PIN6 TS  
PIN7 B/I  
PIN8 BATT+  
PIN9 BATT+  
PIN10 BATT+

---Battery\_Conn\_pin define---

PIN10 Batt+  
PIN9 Batt+  
PIN8 Batt+  
PIN7 B/I  
PIN6 TS  
PIN5 SMC  
PIN4 SMD  
PIN3 GND  
PIN2 GND  
PIN1 GND



For KB9022 OTP	Active	Recovery
VCIN0_PH(V)	92C, 1V	56C, 2V
PH201 (ohm)	7.3K	26.11K

For KB9022 sense 5mΩ	Active	Recovery
330W PR208=95.3Kohm	1V(462W)	1V(462W)

PH201 under CPU bottom side :  
CPU thermal protection at 92 degree C ( shutdown )  
Recovery at 56 degree C

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				Date:	Monday, January 09, 2017
				Sheet	74 of 103



Input Current: 7.5A  
 $3.3V \cdot 10A / 0.85 / 12V = 2.23$   
 $5V \cdot 10A / 0.85 / 12V = 5.27$

Output capacitor ESR need follow below equation to make sure feedback loop stability  
 $ESR = 20mV \cdot L \cdot f_{sw} / 2V$

POK need pull high, it will pull high on VS transfer circuit

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**3.3VALWP**  
 TDC=8.26A  
 Peak Current 11.8A  
 OCP current 14.16A (Pr405=100k)  
 FSW=355kHz

	TYP	MAX
H/S Rds(on)	11.2mohm	14mohm
L/S Rds(on)	6.7mohm	8.5mohm

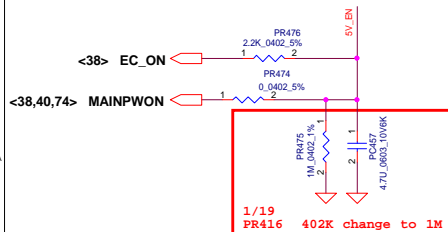
$OVP = V_{out} \cdot (112.5\% \sim 117.5\%)$   
 $OCP = V_{trip} / R_{dson} + I_{ripple} / 2$   
 $V_{trip} = I_{cs(min)} \cdot R_{cs} / 8 + 1mV$   
 $V_{cs} = I_{cs} \cdot R_{cs}$  should be in the range of 0.2~2V  
 $I_{cs} = 9 \sim 11uA$

$V_{out} = V_{FB} \cdot (1 + R_{top} / R_{bot})$   
 $V_{FB} = 2V$

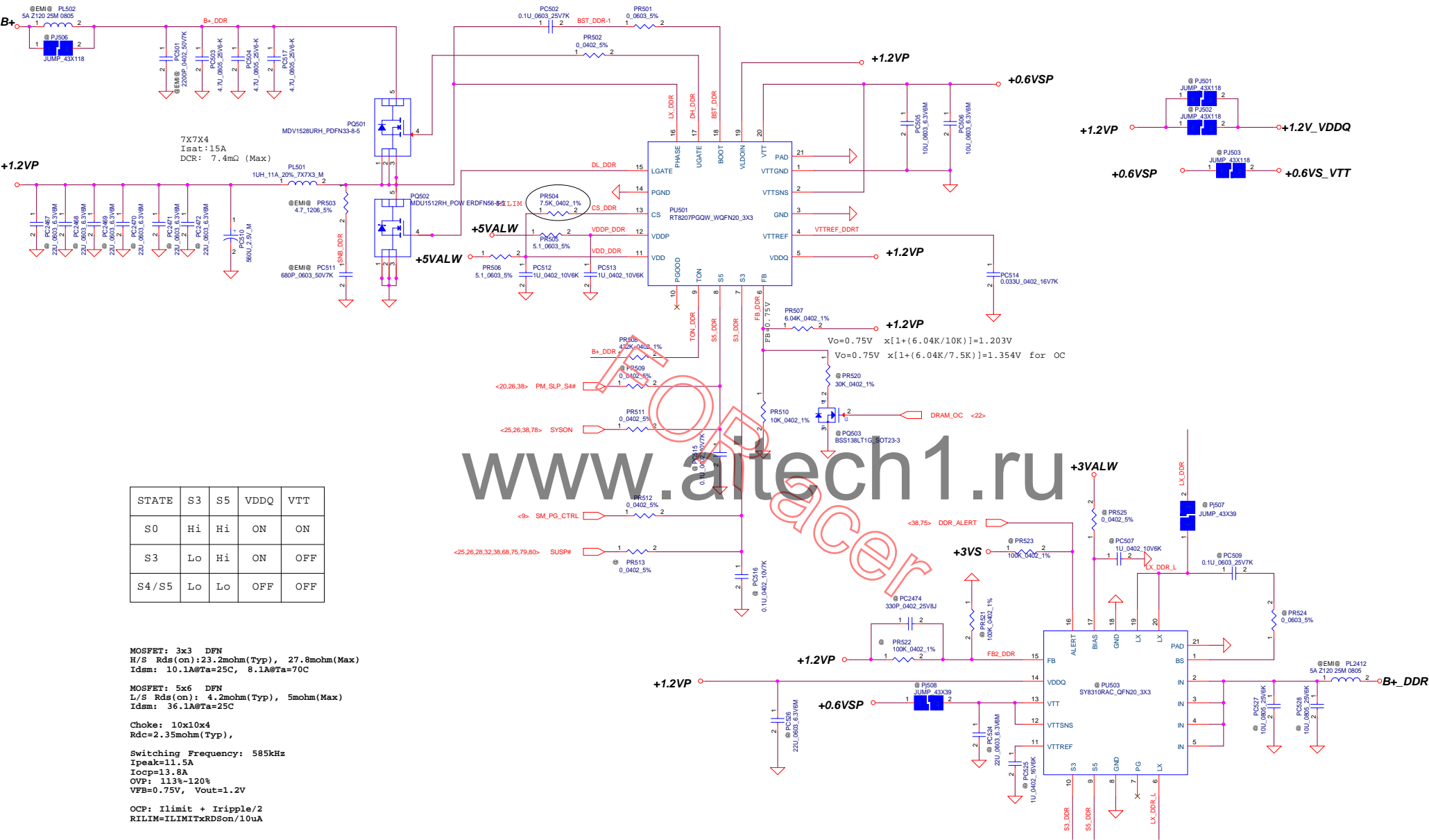
**5VALWP**  
 TDC=15.75A  
 Peak Current 22.5A  
 OCP current 27A (Pr407=97.6k)  
 FSW=300kHz

	TYP	MAX
H/S Rds(on)	11.2mohm	14mohm
L/S Rds(on)	6.7mohm	8.5mohm

ESR = 14mohm



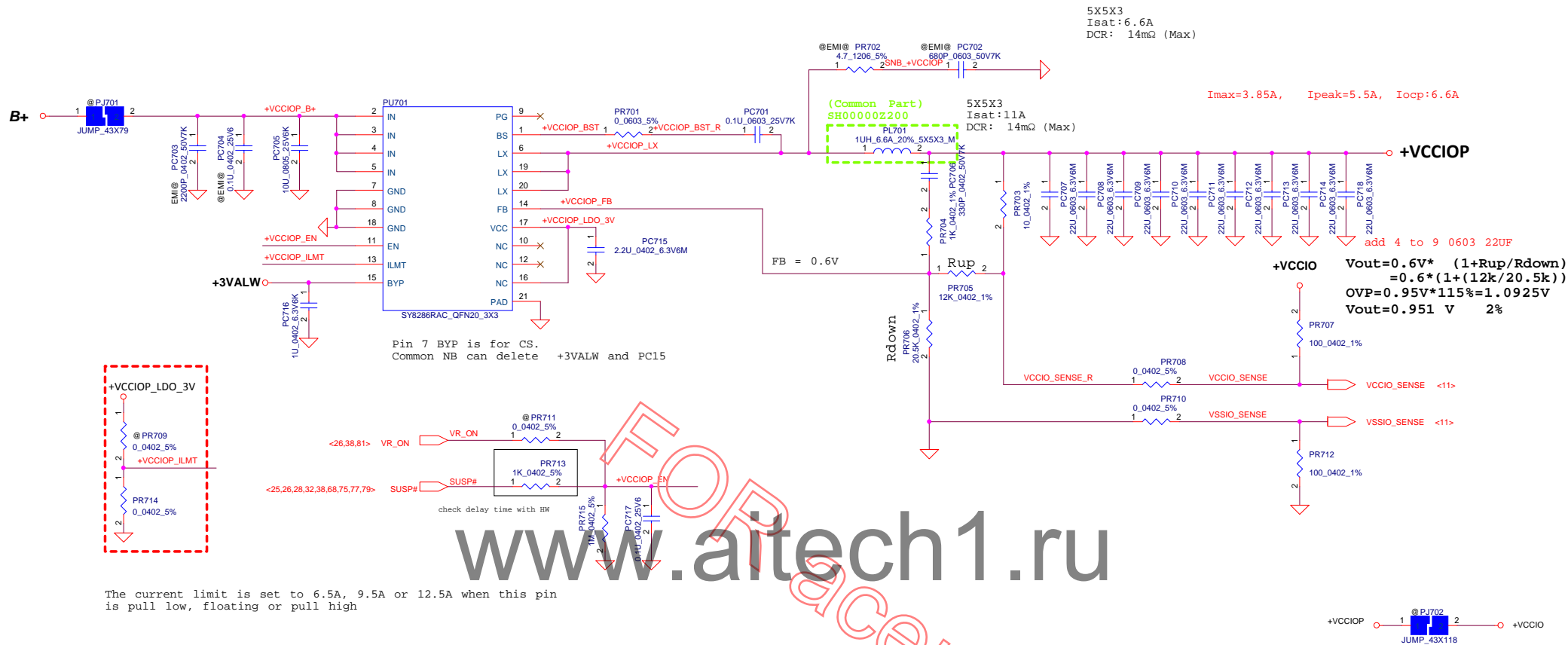
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Size	Document Number	Sheet	76 of 103	Rev 1.0
Date:	Monday, January 09, 2017	Sheet	76 of 103	







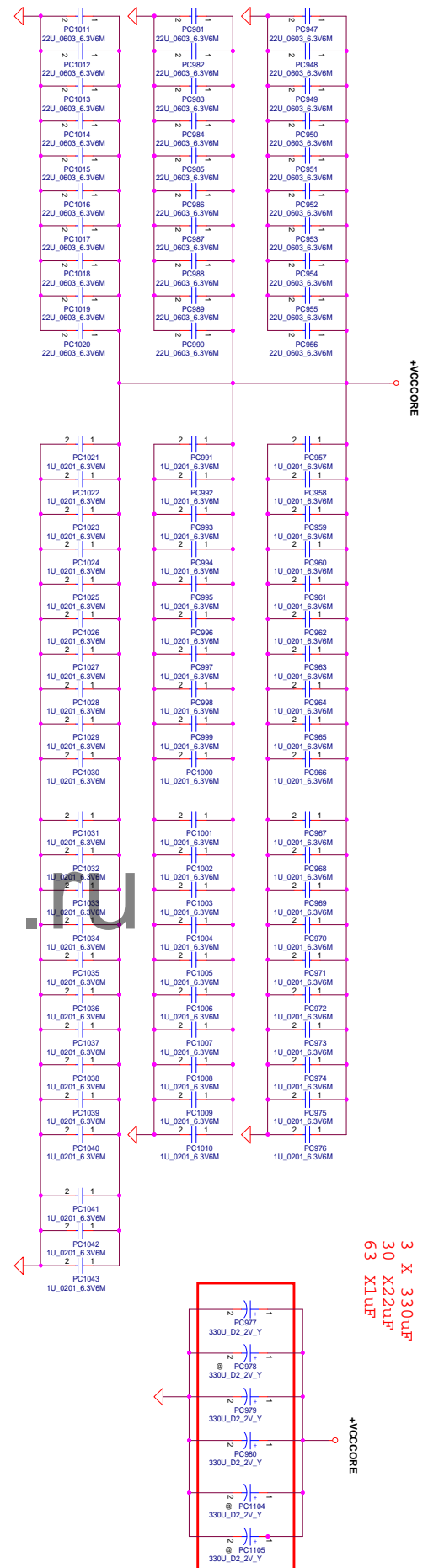




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				Date:	Monday, January 09, 2017	Sheet	80 of 103







Total VCCSA Output Capacitor:  
 3 X 1uF-0201  
 12 X 22uF-0603

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Doc No.	SKL_H 42	Doc No.	SKL_H 42	Doc No.
Rev.	1.0	Rev.	1.0	Rev.
Date:	March, January 09, 2017	Date:	March, January 09, 2017	Date:

Processor decoupling

# Master GPU

layout 上：  
請將 Total I DCR sensing 的 component  
放靠近 Controller.

close phase1

layout 上：請將 RSEN1 ~ 4  
放靠近 Controller.

請教 AUD  
PHASE 的設定

PWMVID 的 RC BOM 標公式  
請根據 GPU's config 設定

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Size	Document Number	Sheet	84	Rev 1.0
C	CIPRG LA-E051P	Monday, January 09, 2017	1	of 103



**Master GPU**



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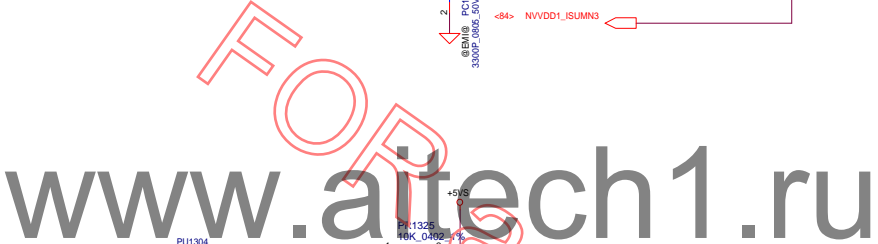
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<b>Compal Electronics, Inc.</b>	
Title	<b>PWR +NVVDD</b>

Size	Document Number	Rev
	SKL_H 42	1.

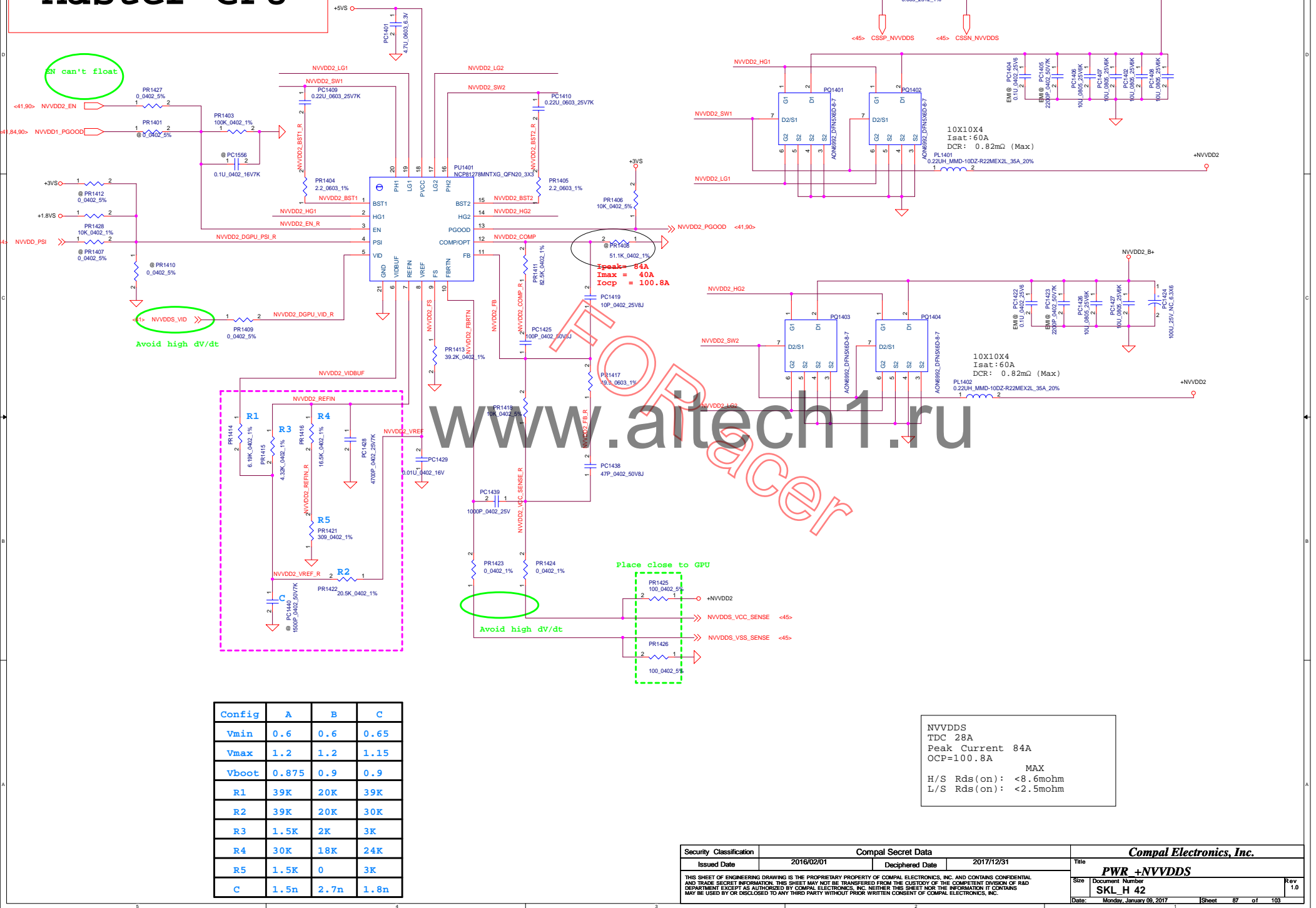
Date:	Monday, January 09, 2017	Sheet	85	of	103
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**Master GPU**



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# Master GPU

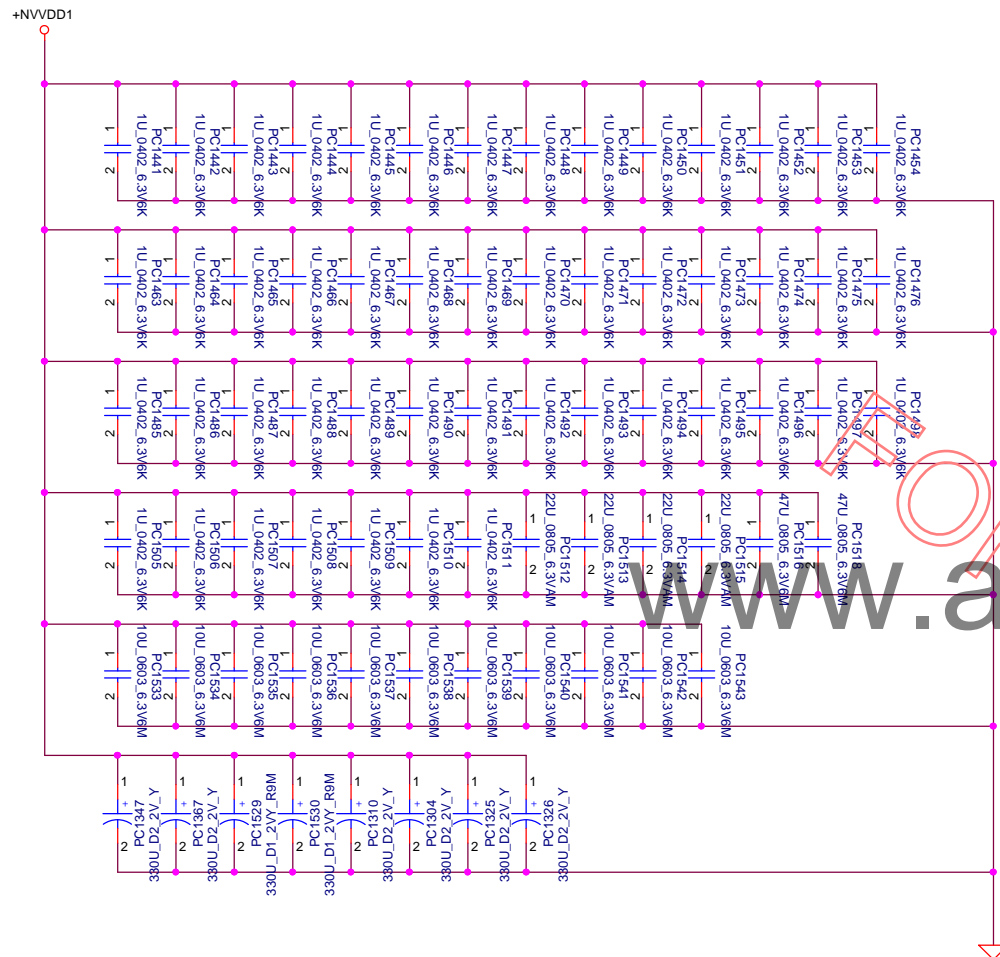


Config	A	B	C
Vmin	0.6	0.6	0.65
Vmax	1.2	1.2	1.15
Vboot	0.875	0.9	0.9
R1	39K	20K	39K
R2	39K	20K	30K
R3	1.5K	2K	3K
R4	30K	18K	24K
R5	1.5K	0	3K
C	1.5n	2.7n	1.8n

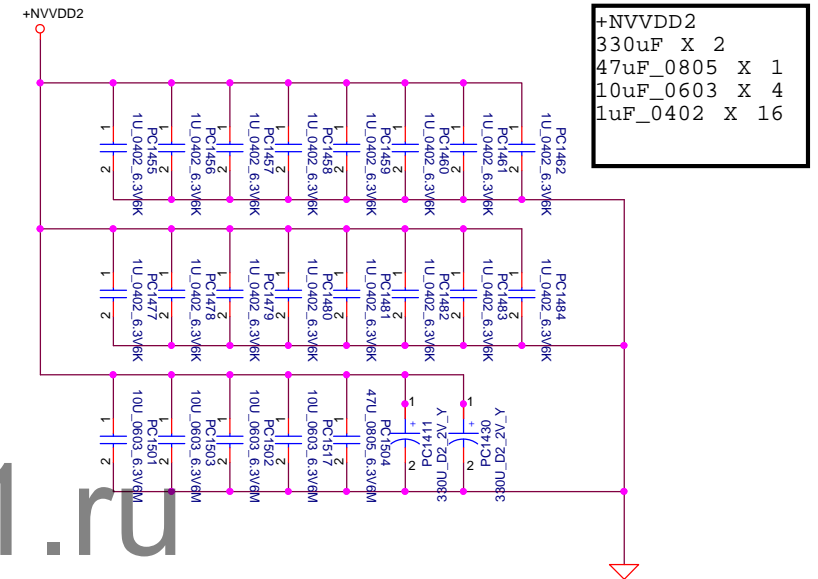
NVVDDS  
TDC 28A  
Peak Current 84A  
OCP=100.8A  
MAX  
H/S Rds(on): <8.6mohm  
L/S Rds(on): <2.5mohm

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				SKL_H 42
				Rev 1.0
				Date: Monday, January 09, 2017
				Sheet 87 of 103

# Master GPU



```
+NVVDD
330uF X 8
47uF_0805 X 2
22uF_0603 X 4
10uF_0603 X11
1uF_0402 X 49
```

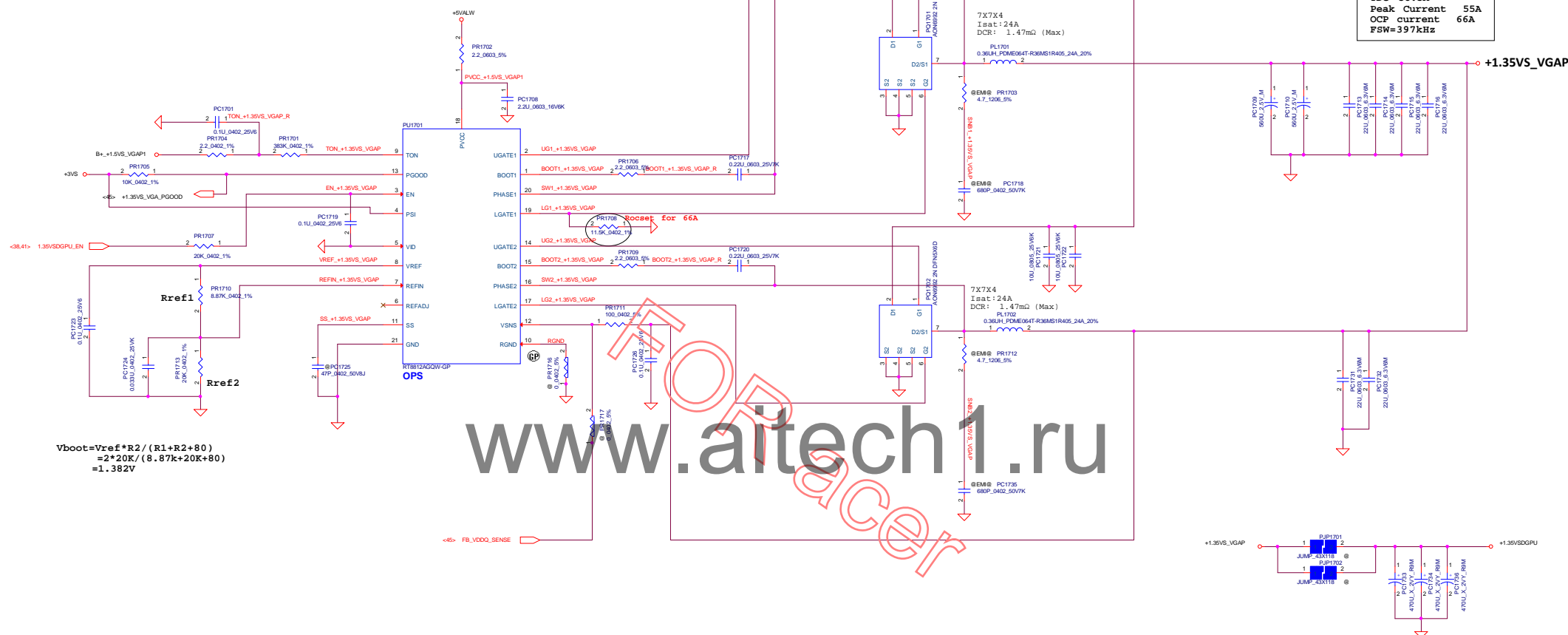


```
+NVVDD2
330uF X 2
47uF_0805 X 1
10uF_0603 X 4
1uF_0402 X 16
```

# Master GPU

+1.5V\_VGAP  
TDC 38.5A  
Peak Current 55A  
OCP Current 66A  
FSW=397kHz

+1.35VS\_VGAP

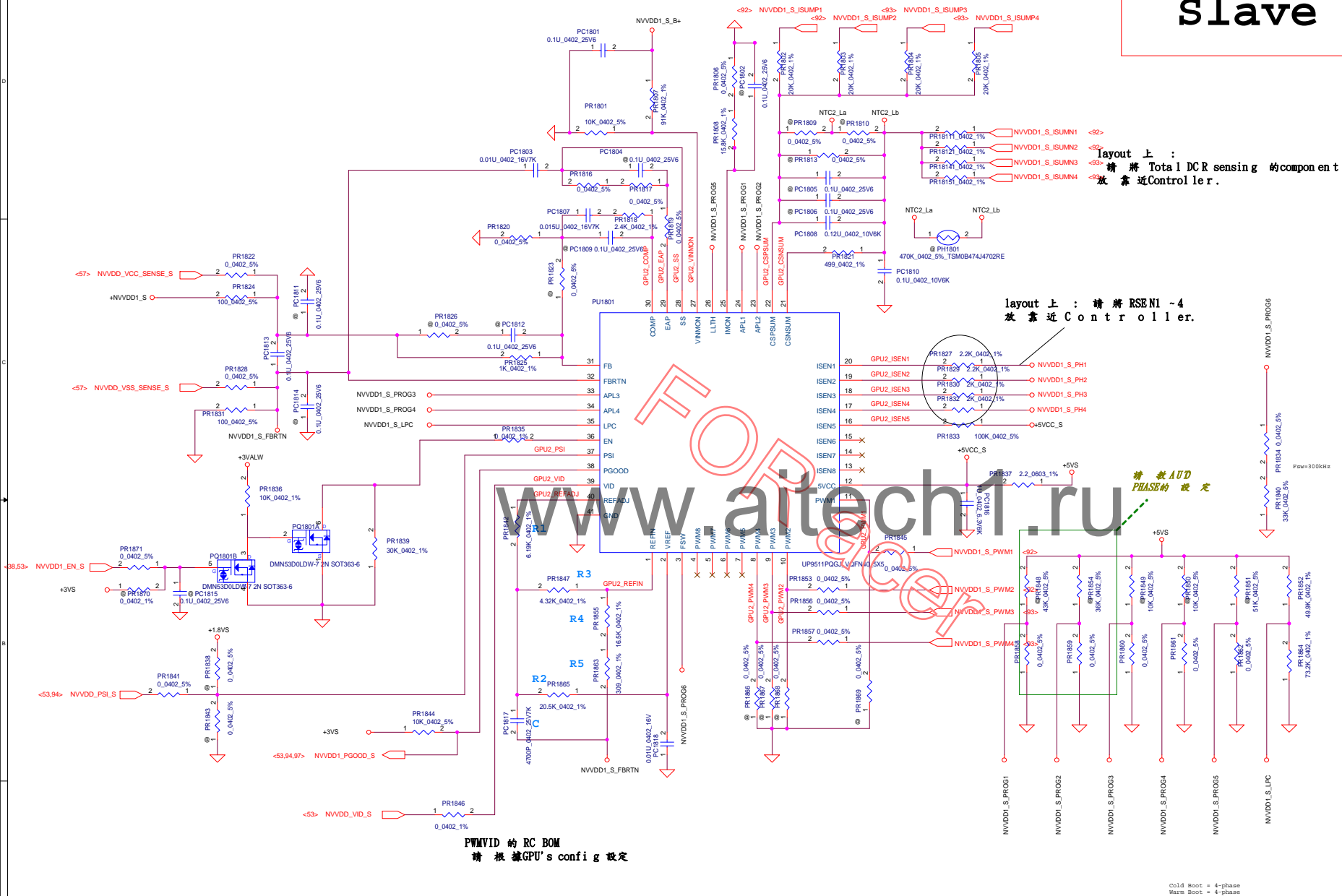


$$V_{boot} = V_{ref} \cdot R_2 / (R_1 + R_2 + 80) \\ = 2 \cdot 20K / (8.87K + 20K + 80) \\ = 1.382V$$

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Site	Document Number	Rev		Rev	
	SKL H 42	1.0		1.0	
Date	Monday, January 09, 2017	Sheet	80	of 103	



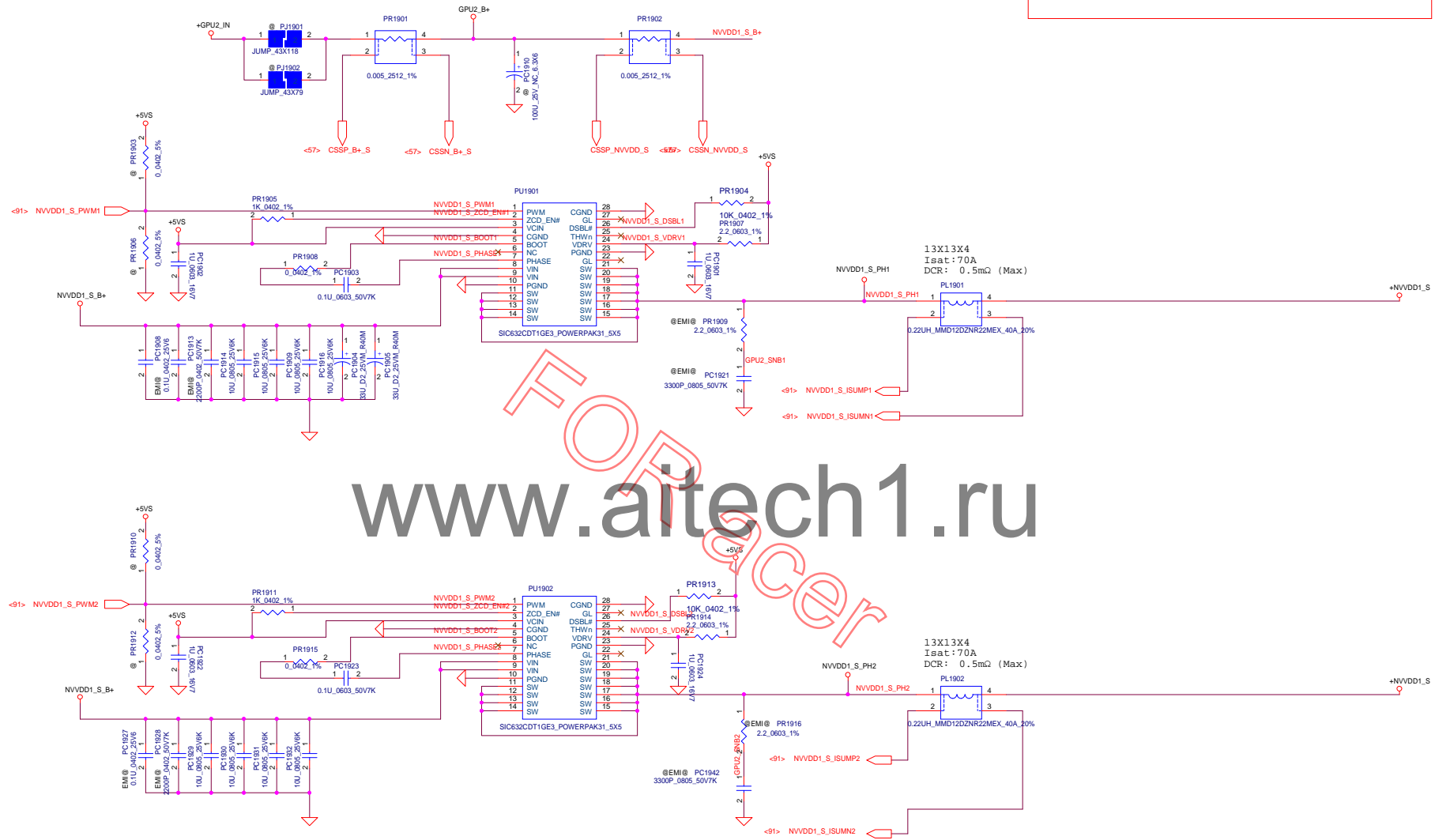
# Slave GPU



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				Document Number
				CIPRG LA-E051P
				Rev
				1.0
Date: Monday, January 09, 2017		Sheet 91 of 103		

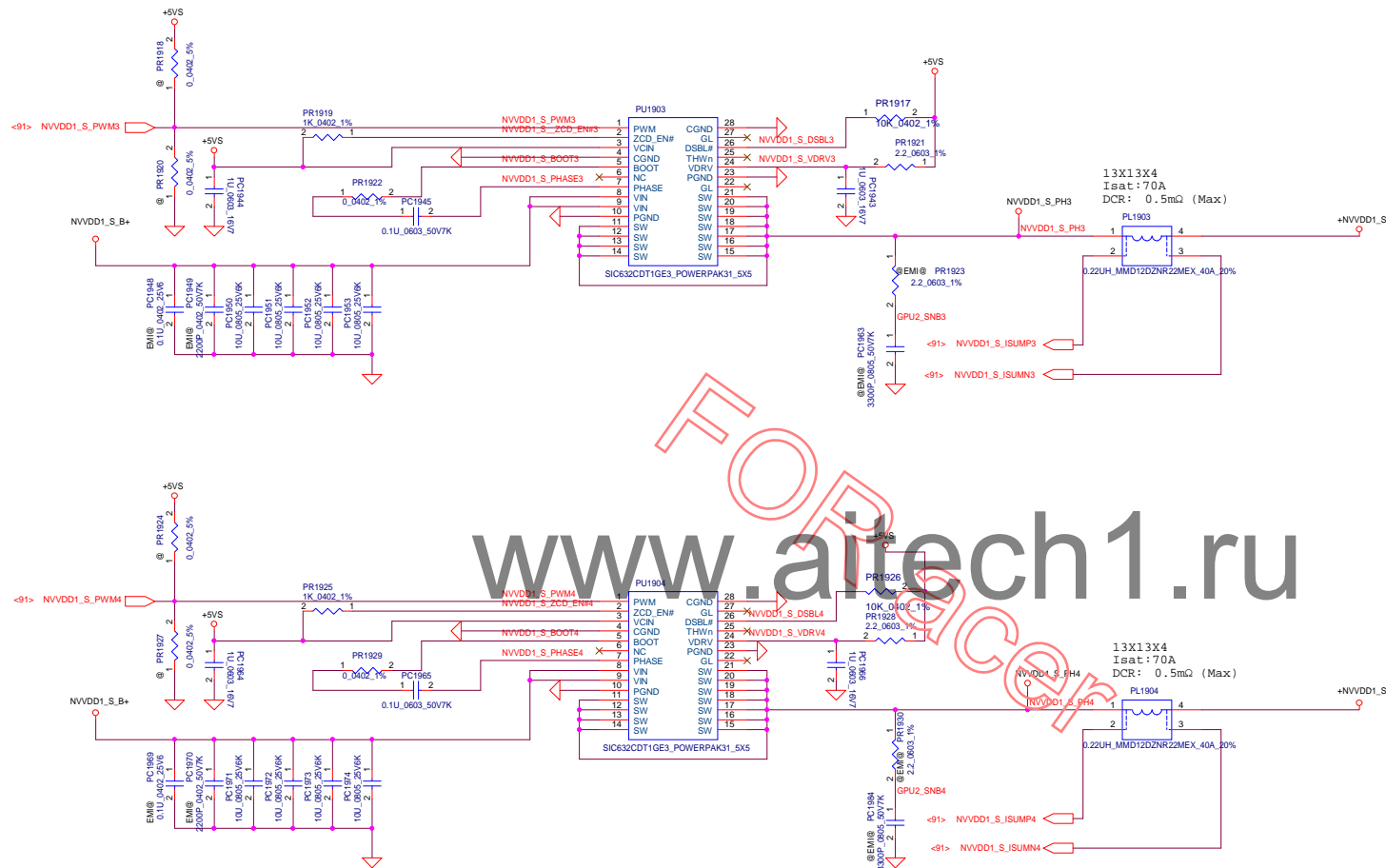


# Slave GPU



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					Rev 1.0
Date: Monday, January 09, 2017					Sheet 92 of 103

# Slave GPU



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				Date: Monday, January 09, 2017	Sheet 83 of 103

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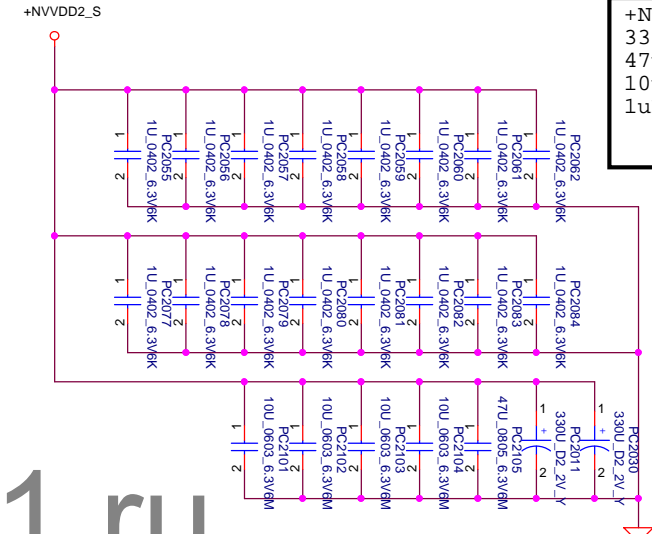
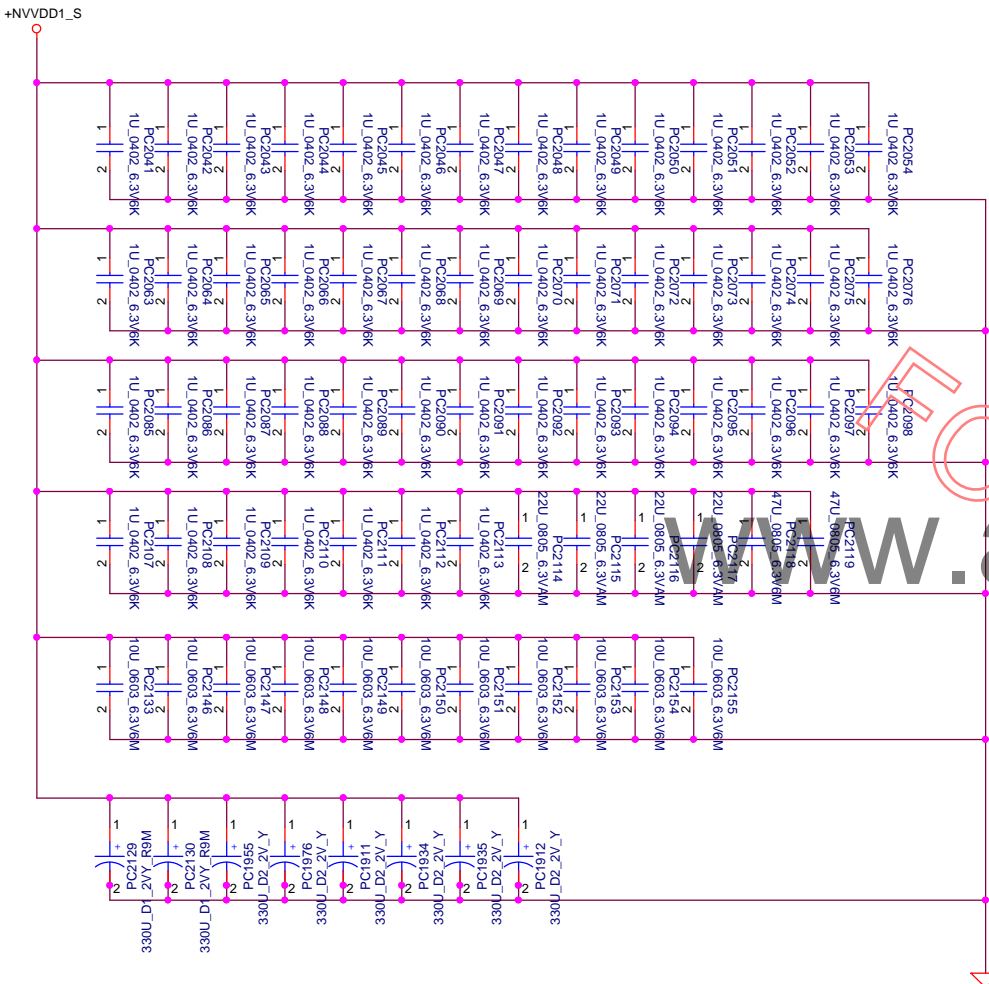
Config	A	B	C
Vmin	0.6	0.6	0.65
Vmax	1.2	1.2	1.15
Vboot	0.875	0.9	0.9
R1	39K	20K	39K
R2	39K	20K	30K
R3	1.5K	2K	3K
R4	30K	18K	24K
R5	1.5K	0	3K
C	1.5n	2.7n	1.8n

NVVDDS	
TDC 28A	
Peak Current 74A	
OCP=89A	
	TYP MAX
H/S Rds(on):	6.7mohm , 8.5mohm
L/S Rds(on):	1.8mohm , 2.3mohm

# Slave GPU

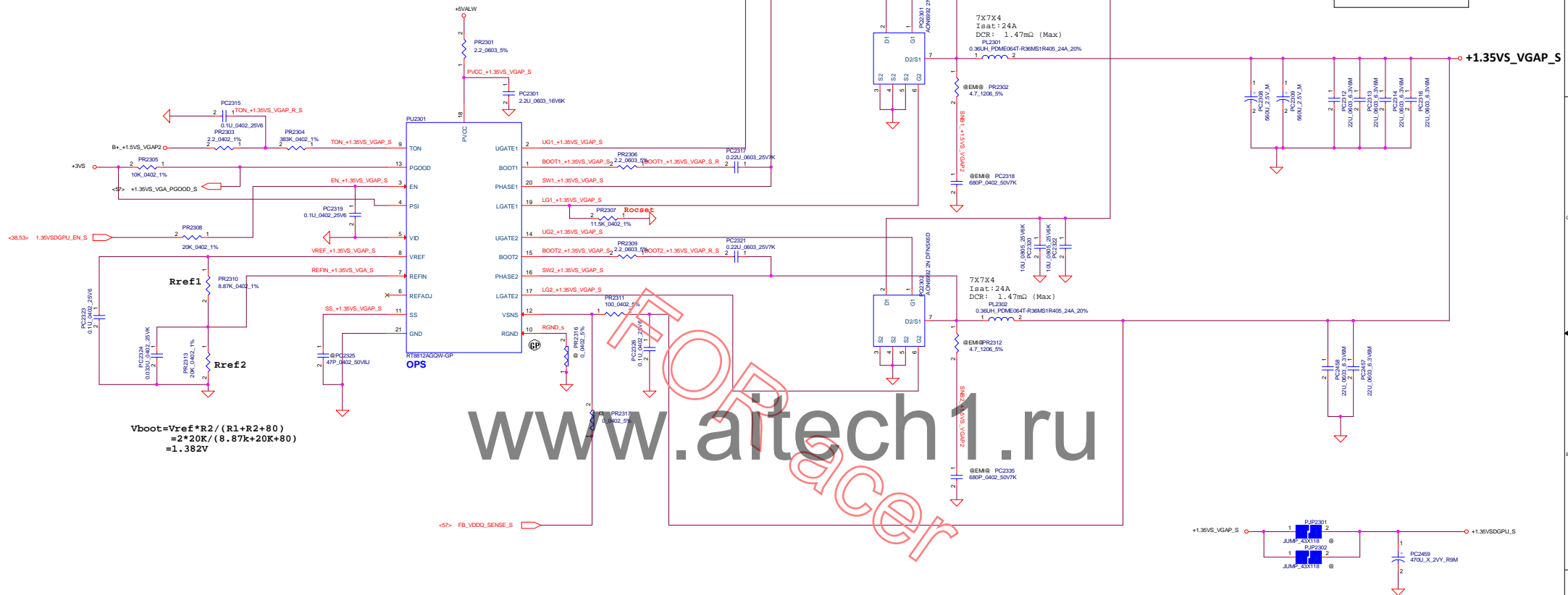
+NVVDD1\_S  
330uF X 8  
47uF\_0805 X 2  
22uF\_0603 X 4  
10uF\_0603X 11  
1uF\_0402 X 49

+NVVDD2\_S  
330uF X 2  
47uF\_0805 X 1  
10uF\_0603 X 4  
1uF\_0402 X 16



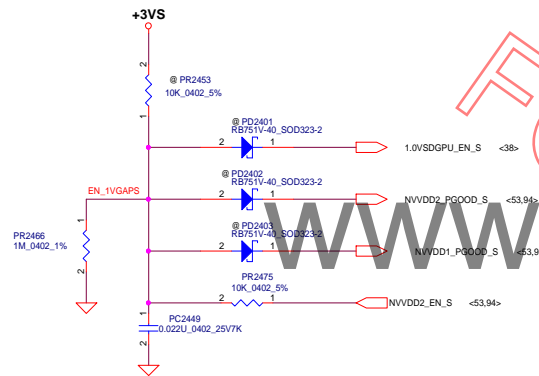
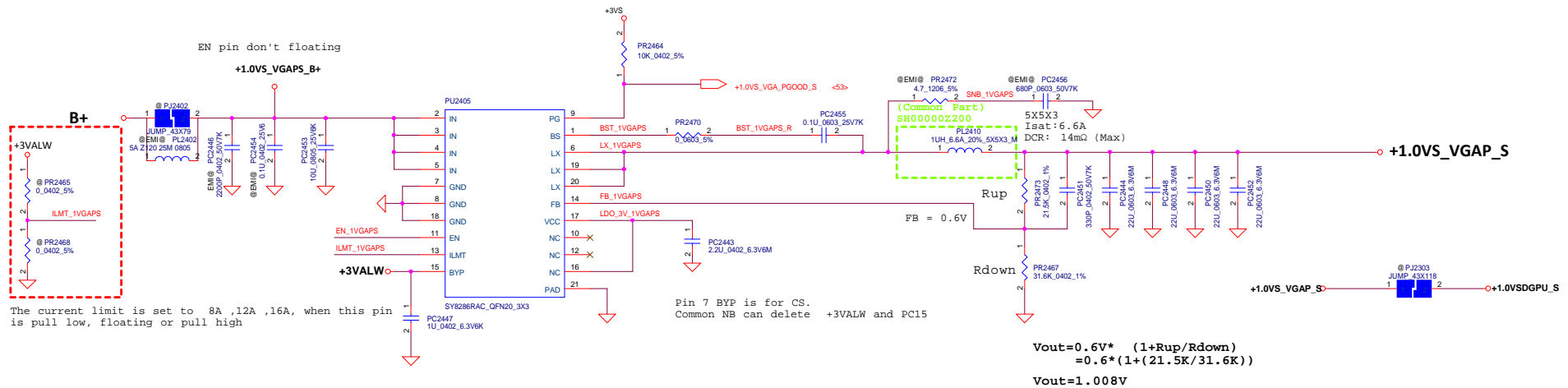
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Issued Date	2016/02/01	Deciphered Date	2017/12/31	Title	
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				Size	Document Number
				C1PRG LA-E051P	
				Date:	Monday, January 09, 2017
				Sheet	95 of 103

# Slave GPU



$$V_{boot} = V_{ref} \cdot R_2 / (R_1 + R_2 + 80) = 2 \cdot 20K / (8.87K + 20K + 80) = 1.382V$$

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2016/02/01	Deciphered Date	2017/12/31	Title	PWR +1.5VRAM
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Rev	Document Number	SKL H 42		Date	Monday, January 05, 2017
1.0				Sheet	96 of 103



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Issued Date	2016/02/01	Deciphered Date	2017/12/31	Title	
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				Size	Document Number
				SKL_H 42	Rev 1.0
				Date: Monday, January 09, 2017	Sheet 97 of 103

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P72	non-POP	7/20	Jims_Liu	AC_IN1 & AC_IN2 output level for one shot sequence	PD101 & PD104(SC400001200) change form POP to non-POP	
2	P72	change	7/20	Jims_Liu	reduce inrush current	PU102 pin8 VCC change from +5V5 to +5VALWP	
3	P73	non-POP	7/20	Jims_Liu	keep AC_in2 voltage 3V	PC114 change to non-POP	
4	P73	change	7/20	Jims_Liu	SPOK pull high	PR125 change from 0 to 100kohm_SD028100380	
5	P76	Add	7/20	Jims_Liu	rise 5valw level to 5.1V	Add PR401_100kohm_SD028100380	
6	P76	change	7/20	Jims_Liu	for NVVDD1 ENable sequence	PR402 change from 15k to 15.4kohm_SD034154280	
7	P84	change	8/3	Jims_Liu	for NVVDD2 response	PR1236 pull high voltage, change from +3VSDGPU to +3VALWP PR1270 pull high voltage, change from +3VSDGPU to +3VS	
8	P87	change	7/20	Jims_Liu	not support OC	PC1419 change from 0.01u to 10pF_SE00000F180 PC1425 change from 0.1u_0603 to 100pF_SE07110180_0402 PC1428 change from 1500pF to 4700pF_SE075472K80	
9	P89	delete	7/20	Jims_Liu	rise 1.35V level to 1.38V	Delete PR1715, PC1736,PQ1703,PR1714	
10	P89	change	7/20	Jims_Liu	for NVVDD1_S ENable sequence	PR1710 change from 10k to 8.87k ohm_SD034887180 PR1713 change from 34.8k to 20k ohm_SD034200280	
11	P91	non-POP	8/3	Jims_Liu	for NVVDD2_S response	PR1836 pull high voltage, change from +3VSDGPU_S to +3VALW PR1870 pull high voltage, change from +3VSDGPU_S to +3VS	
12	P94	change	7/20	Jims_Liu	not support OC	PC2019 change from 0.01u to 10pF_SE00000F180 PC2026 change from 0.1u_0603 to 100pF_SE07110180_0402 PC2028 change from 1500pF to 4700pF_SE075472K80	
14	P96	delete	7/20	Jims_Liu	rise 1.35V level to 1.38V	Delete PR2315, PC2336,PQ2303,PR2314	
15	P96	change	7/20	Jims_Liu	DFB issue	PR2310 change from 10k to 8.87k ohm_SD034887180 PR2313 change from 34.8k to 20k ohm_SD034200280	
16	P90	delete	7/20	Jims_Liu	charger I limit	delete PC1601_2200pF_EMI	
17	P75	change	8/11	Jims_Liu	HW PSI pin combine	PR314 change from 20k_SD034200280 to 392k_SD034392380 PR316 change from 2k_SD034200180 to 25.5k_SD034255280 PR315 change from 52.3k_SD034523280 to 715k_SD034715380	
18	P87	change	7/26	Jims_Liu	HW PSI pin combine	PR1407 pin1 change from NVVDD5_PSI to NVVDD_PSI	
19	P94	change	7/26	Jims_Liu	HW request	PR2007 pin1 change from NVVDD5_PSI_S to NVVDD_PSI_S	
20	P90	non-POP	7/26	Jims_Liu	HW request	PD1601 PD1603 PR1607 change to non-POP	
21	P90	change	7/26	Jims_Liu	HW request	PR1608 change to POP 10k_SD028100280	
22	P97	non-POP	7/26	Jims_Liu	HW request	PD2401 PD2403 PR2453 change to non-POP	
23	P97	change	7/26	Jims_Liu	HW request	PR2475 change to POP 10k_SD028100280	
24	P84	change	7/26	Jims_Liu	change sequency	PR1244 change to POP 10k_SD028100280 and pull high change from +3VSDGPU to +3VS	
25	P91	change	7/26	Jims_Liu	for Transient test	PR1844 change to POP 10k_SD028100280 and pull high change from +3VSDGPU_S to +3VS	
26	P79	Add	7/28	Jims_Liu	for Transient test	Add PC2208_22uF_SE00000M000	
27	P89	POP	7/28	Jims_Liu	for ACOK signal quality	PC1710_560uF_SF000002P00 change to POP	
28	P72	change	8/2	Jims_Liu	HW request change Vth to 1.8V	PU102 pin8 & pin1 & pin7 VCC change from +5VALWP to +19V_ref PR124 & PR118 change from 1.5M to 16.9k_SD034169280	
29	P84	change	8/2	Jims_Liu	HW request change Vth to 1.8V	PQ1201 change from 2N7002_SB00000E000 to DMN53D_SB000018X00	
30	p91	change	8/2	Jims_Liu	mos 30A	PQ1801 change from 2N7002_SB00000E000 to DMN53D_SB000018X00	
31	P75	change	8/3	Jims_Liu	NV suggest	PQ301 & PQ304 change from A0N6426_SB000017800 to MDU1512_SB000005Y00	
32	P84	change	8/3	Jims_Liu	NV suggest	PC1217 change from 1500p_SE074152K80 to 4700p_SE075472K80	
33	P84	change	8/3	Jims_Liu	change common part	PC1817 change from 1500p_SE074152K80 to 4700p_SE075472K80	
34	P80	change	8/3	Jims_Liu	dynamic FAN 9V	PL701 change from 1uH_SH00000NW00 to 1uH_SH00000Q200	
35	P78	add	8/3	Jims_Liu	for FAN_12V ripple	add PR2447_280k_SD034280380, PQ2411_2N7002_SB00000ST00	
36	P78	add & delete	8/3	Jims_Liu	for FAN_12V ripple	delete PC2435_33u_SGA00007100, add PC2439 & PC2475 & PC2438_22u_SE00000GB5Q	
37	P78	change	8/4	Jims_Liu	change common part	PC2436 change from 47PF to 1000P_SE00000H180 PR2435 change from 56.2k to 19.6k_SD000003580	
38	P76	change	8/4	Jims_Liu	change common part	PC407 & PC409 & PC410 change from 330u_SF000001G00 to 330u_SF000006B00	
39		change	8/4	Jims_Liu	change common part	PC928,PC929,PC930,PC1309,PC1424,PC1910,PC2009,P change from 100u_SF000005100 to 100u_SF000007100	
40	P82	change	8/4	Jims_Liu	for buyer	PL901,PL903,PL904,PL906 change from 0.22u_SH00000NM00 to 0.22u_SH00000QZ00	
41		change	8/4	Jims_Liu	NV recommend	EMI bead PL101,PL102,PL103,PL104,PL105,PL106,PL107,PL108,PL109,PL110,PL201,PL202,PL203,PL2404 change from SM01000C000 to SM01000P200	
42	p87	change	8/4	Jims_Liu	NV recommend	PR1425 PR1426 change from 10ohm_SD028100A80 to 100ohm_SD028100080	
43	P94	change	8/4	Jims_Liu	NV recommend	PR2025 PR2026 change from 10ohm_SD028100A80 to 100ohm_SD028100080	
44	P77	add	8/4	Jims_Liu	FAE recommend	add PJ507, PJ508, PL2412,PC2474	
45	p87	change	8/9	Jims_Liu	FAE recommend	PC1440 1500pF_SE074152K80 change to UNPOP PR1421 change from 330ohm_SD028330080 to 309ohm_SD000017700	
46	P87	change	8/9	Jims_Liu	FAE recommend	PC2040 1500pF_SE074152K80 change to UNPOP PR2021 change from 330ohm_SD028330080 to 309ohm_SD000017700	
47	P78	change	8/11	Jims_Liu	for over shoot & output ripple	PC2428 change from 0.1u_SE00000G880 to 0.47u_SE000002F80 PC2425 change from 100u_SGA00006B00 to 22u_SE00000GB5Q Add PC2421 & PC2422 22u_SE00000GB5Q	
48	P75	change	8/11	Jims_Liu	change size & common part	PL301 change from 10x10 4.7uH_SH00000HR00 to 7x7 4.7uH_SH00000YC00	
49	P72	change	8/11	Jims_Liu	change voltage rating	PC109 & PC110 change from 0.022u_16V_SE076223K80 to 0.022u_25V_SE075223K80	
50	P74	unpop	8/12	Jims_Liu	thermal requirement	PH202 & PH202 change to unpop	
51	P96	POP	7/28	Jims_Liu	for Transient test	PC1710_560uF_SF000002P00 change to POP	
52	P78	add & delete	8/19	Jims_Liu	for FAN_12V ripple	PC2421, PC2422, PC2425, PC2438, PC2439, PC2475 change from SE00000GB5Q to SE00000GB00	
53	P72	change	8/24	Jims_Liu	for one shot discharge	PR116 & PR117 change from 47k_SD034470280 to 470k_SD034470380 PR118 & PR124 change from 16.9k_SD034169280 to 169k_SD034169380 PC109 & PC110 change from 0.022u_SE075223K80 to 0.22u_SE000015W00 PC2436 change from 1000pF_50V_SE00000H180 to 1000p_SE068102180_25V	
54	P78	change	8/24	Jims_Liu	for buyer	Add PC120, PC121, PC122, PC123 0.1uF_SE042104K80	
55	P72	add	10/18	Jims_Liu	for EMI	Add PC124 0.1uF_SE00000G880_unpop	
56	P73	add	10/18	Jims_Liu	for AC_in	PC112 change to UNPOP	
57	P73	pop	10/18	Jims_Liu	for AC_in	PQ116 change to B2B.	



Title		eTitle	
Line	Description	Quantity	Unit
1	Office		
Date		Month	Year
		January	2017

Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
1	32,38	EC	7/11	Change LED design and update EC GPIO.	1. Remove PWR_SUSP_LED#/ BATT_AMB_LED#/ BATT_AMB_LED#/ PWR_LED from U28, add EC_SMB_CK3/ EC_SMB_DA3 for 2nd 59116 on USB/B. 2. Add SATA_LED# to pin93,move BT_ON to pin108, move FW_GPIO to pin 90.	DVT	0.2
2	32	USB	7/11	TI USB3.0 re-driver no function	1. Del USB3.0 re-driver circuit. U10,C443~C446,R3,R118~R120,R407,R408.	DVT	0.2
3	22	PCH	7/11	Leakage issue.	1. unpop RH143.	DVT	0.2
4	23	PCH	7/11	RTC BATT use non-chargeable type.	1. Add RH163, change DH2 PN.	DVT	0.2
5	41,45, 53,57	GPU	7/11	Change GPU power sequence by HW control.	1. unpop RG780, pop RG779. 2. unpop RG515/RG784, pop RG783. 3. unpop RG789, pop RG792, change RG768 to 20k. 4. unpop RG782, pop RG781. 5. unpop RG604/RG786, pop RG785. 6. unpop RG791, pop RG793, change RG770 to 20k.	DVT	0.2
6	27,32, 35,36	CONN	7/18	ME change connector.	1. JSPK1/JSPK2 change to 8 pin conn SP020010D00. 2. JDMIC1 change to SP020008V00 (pitch change to 1mm). 3. JHDD1 change to SP010022I00. 4. JFANBL change to SP020008R00. 5. JPWRB & JBTN change to SP02000IT00. 6. JUSB2 change to SP01001BY00. 7. JUSB3 change to SP01001I300.	DVT	0.2
7	49~52, 61~64	GPU	7/18	Change VRAM MEM_VREF MOS PN.	1. QG2~4/QG8/QG513~516 change to SB000010N00.	DVT	0.2
8	39	FAN	7/19	FAN power rail.	1. Change JFAN3 power from 12V to 5V.	DVT	0.2
9	25	Jump	7/19	Change jump size.	1. Change J15/J16 from 43*79 to 43*118.	DVT	0.2
10	38	EC	7/19	EC debug.	1. Del T71~T74, replace by R799,R800.	DVT	0.2
11	34	Camera	7/19	TI USB3.0 re-driver no function	1. Del USB3.0 re-driver circuit. U44,C393~C396,C409~C411,R360~R366,R116,R117.	DVT	0.2
12	19,22	PCH	7/19	EC_SCI# change GPIO pin.	1. Move EC_SCI# from GPP_G3 to GPP_B20.	DVT	0.2
13	35	CONN	7/22	Symbol pin definition	1. JFANBL pin reverse for new conn definition	DVT	0.2
14	36	Codec	7/22	Reserve SPDIF_OUT.	1. Reserve RA81, add RA82 for SPDIF_OUT.	DVT	0.2
15	21,68	Crystal	7/22	Crystal EA.	1. Change YH1 to SJ10000Q400. 2. Change CH13 to 8.2pF/ CH14 to 6.8pF. 3. Change C293/C294 to 10pF.	DVT	0.2
16	20	PCH	7/22	Follow design guide.	1. unpop CH67.	DVT	0.2
17	31	M.2	7/22	UART debug.	1. Pop R64,R65.	DVT	0.2
18	38	EC	7/22	Board ID.	1. Change R193 to 12k, pop R191.	DVT	0.2
19	32,35,36	CONN	7/25	Symbol pin definition	1. Reverse JUSB3, JDMIC1, swap JSPK1 pin.	DVT	0.2
20	48,60	GPU	7/25	Add netname for MIO.	1. Add netname for MIO.	DVT	0.2
21	34	CONN	7/25	Correct netname.	1. JCAM2 pin6 connect to +3VS.	DVT	0.2
22	41,45,53, 57,60,66	GPU	7/26	Sequence finetuning and power sequence correct connection	1. Change UG10,UG23 to SA00003R000. 2. Remove RG520,RG521,RG503,RG523,RG556,RG531. 3. Add UG101,CG916,RG797,UG102,CG919,RG798,DG23,RG795,DG24,RG796. 4. Reserve CG917,CG918,CG920,CG921. 5. Pop RG787,RG790. 6. Depop UG99,CG910,CG911,RG771,UG100,CG912,CG913,RG772. 7. Change RG4,RG526 to 0402 size.	DVT	0.2

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				Custom	C1PRG LA-E051P
				Date:	Monday, January 05, 2017
				Sheet	100 of 103
				Rev	1.0

Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
					8. Change RG767,RG769 to 20k. 9. Change RG768,RG770 to 15k. 10. Change RG71,RG593 to 4.7k. 11. Change QG6,QG7,QG501,Q31 Gate pin to DGPU_PEX_RST#_G. 12. Change QG520,QG521,QG522 Gate pin to DGPU_PEX_RST#_S_G. 13. Remove net NVVDDS_PSI, MEM_VDD_CTL, NVVDDS_PSI_S, MEM_VDD_CTL_S. 14. Change Q31 to SB000016K00. 15. Change RP3 pin6,7 to +1.8VSDGPU_MAIN. 16. Correct MIOA CLK connect i on		
23	32	CONN	7/26	CONN symbol pin def i ne	1. Swap JUSB2 pin for USB3.0 port 2. Swap JUSB3 pin for USB3.0 port 4.	DVT	0.2
24	26	Sensor	7/27	External termal sensor design.	1. Remove C827, add R801, change R798 to 10k.	DVT	0.2
25	35	CONN	7/27	ME change connector.	1. Change JLB1 to 16pin connector(SP02000I900).	DVT	0.2
26	47,59	Crystal	7/27	Change PN.	1. Change YG1,YG2 to SJ10000DK00.	DVT	0.2
27	32	CONN	7/29	CONN symbol pin def i ne	1. Reverse JUSB3 and swap USB pin.	DVT	0.2
28	41,53	GPU	7/29	For layout placement.	1. Change DG1,DG8 to SOT-323 symbol.	DVT	0.2
29	32	CONN	8/2	CONN symbol pin def i ne	1. Swap JUSB3 for USB3.0 port 5.	DVT	0.2
30	35	CONN	8/2	CONN symbol pin def i ne	1. Reverse JLB1.	DVT	0.2
31	70	CONN	8/2	ME change connector.	1. Change JUSB1 connector.	DVT	0.2
32	28	M.2	8/2	For layout placement.	1. Change CN23 to B2 size(220uF).	DVT	0.2
33	38	EC	8/3	Update EC GPIO.	1. Change DDR_ALERT connect to EC pin92. 2. Add FAN_9V net on EC pin34.	DVT	0.2
34	27,40	symbol	8/4	Update symbol.	1. Update U7(SATA redriver) symbol, U31(TPM) symbol.	DVT	0.2
35	40	CONN	8/4	ME change connector.	1. Change JLID1 symbol.	DVT	0.2
36	41,45,47, 53,57,59, 66	GPU	8/5	NV review.	1. Change QG5 pin5 connect i ont o +1 8VS DGPU_ MA N 2. Change netname NVVDD2_EN_R to NVVDD2_EN_R1. 3. Change QG517 pin5 connect i ont o +1 8VS DGPU_ MA N_S 4. Change RG598,RG619 to 10k. 5. Change RG76,RG626 to 0ohm. 6. Change UG13 VDD to +1.8VSDGPU_AON. 7. Change UG35 VDD to +1.8VSDGPU_AON_S. 8. Change RP3 pin6,7 connect i ont o +1 8VS DGP U_AON 9. Add RV27~RV34,RG799~RG804.	DVT	0.2
37	41,66,68	GPU	8/9	NV review.	1. Pop RG517. 2. Change RG688 to 0ohm. 3. Add R802,R803. 4. Remove RX1.	DVT	0.2
38	35,40	LID	8/9	ME change design.	1. Remove JLID1, move LID_SW# net to JPWR.	DVT	0.2
39	70	USB	8/10	CONN GND shelding.	1. Add H35~H40(2P4X0P9 PTH).	DVT	0.2
40	66	GPU	8/11	NV review.	1. Add RV35~RV42.	DVT	0.2
41	36	EMI	8/11	EMI test.	1. Reserve RA83,RA85,CA78,CA79, add RA86, pop CA32.	DVT	0.2
42	66	GPU	8/11	For layout rout i ng	1. Swap VGA_TMDS_TX2N/P for rout i ng s not H y	DVT	0.2
43	36	Codec	8/11	Correct connect i on and S MBus EA	1. Change RA82 connect i ont o SPDF_OUT 2. Change RA21,RA23 to 4.7k.	DVT	0.2
44	36	EMI	8/15	EMI test.	1. Remove RA86, add LA15 and correct connect i on 2. Pop RA83,RA85 to 100 ohm. 3. Pop CA78,CA79 to 330pF.	DVT	0.2

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				Custom	C1PRG LA-E051P
				Date:	Monday, January 05, 2017
				Sheet	101 of 103

Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
45	23	PCH	8/16	Change PN.	1. Change DH2 to SC600000B00.	DVT	0.2
46	38	GPU	8/16	Sequence by HW control.	1. Unpop UE5,R385,R399,C436,CE3.	DVT	0.2
47	26	Sensor	8/17	Change PN.	1. Change C823 to SE076104K80. 2. Change U52 to SA00003PU00.	DVT	0.2
48	47,59	GPU	8/17	Update straps set ting for G sys	1. Pop RG83, unpop RG95. 2. Unpop RG628, pop RG610.	DVT	0.2
49	41,53	GPU	8/17	Change PN.	1. Change UG22,UG24 to SA000000H00.	DVT	0.2
50	38,39	FAN	10/11	Change FAN def i ne	1. Swap JFAN1,JFAN3 and netname. 2. Change JFAN1 symbol to SP02000TI00.	PVT	0.3
51	38	EC	10/11	Change board ID.	1. Change R193 to 15k.	PVT	0.3
52	22,34 38	CAM	10/11	Remove 3D CAM.	1. Remove JCAM2,U18,R419,C114,C115,C118,C439,C440,R386,R387. 2. Reserve T71~T74.	PVT	0.3
53	33	POGO	10/11	Add protect circuit.	1. Add Q37,R804,R805.	PVT	0.3
54	28	LED	10/11	Add storage LED circuit.	1. Add U71,U72,U73,RN18,RN19. Reserve RN20. Remove RA81,RA82.	PVT	0.3
55	38,70	I2C	10/11	Change I2C power rail for BATT LED.	1. Remove R317,R318. 2. Change R428,R429 to 4.7k and PU to +5VALW. 3. Add Q38,R806,R807.	PVT	0.3
56	35	LED	10/17	Change LED driver power rail.	1. Change UE3 power source from +3VALW to +5VALW.	PVT	0.3
57	32,38	LED	10/17	Add LED power control.	1. Add LEDPWR_EN net, connect JUSB3.17 and U28.90. 2. Reserve T75,T76.	PVT	0.3
58	65	Panel	10/25	Panel design change.	1. Change LCD_OD PU to +3VS for panel side. 2. Pop Q29,R406.	PVT	0.3
59	65	Panel	10/25	Panel DC S5 mode power consumpt i on issue	1. Reserve L15, Q39, Q40, R808, R809, C824.	PVT	0.3
60	32	IO/B	10/25	Change IO/B CONN pin def i n i t i o n	1. Remove USB port3. 2. Change JUSB2 pin def i n i t i o n	PVT	0.3
61	59	ROM	10/27	Avoid GPU ROM part mixed.	1. Change UG35 to SA00009ZQ00.	PVT	0.3
62	68	TBT	10/27	Change TBT to C1 step.	1. Change U36 to SA00009YL60.	PVT	0.3
63	37	AMP	10/27	Update AMP PN.	1. Change UA2,UA3 to SA00008AG10.	PVT	0.3
64	38	EC	10/28	For OVP test.	1. De-pop D16.	PVT	0.3
65	35	LED	10/31	For LED brightness.	1. Change RE23,RE24,RE27,RE28,RE31,RE32,RE15,RE17,RE19 to 4.7kohm. 2. Change RE21,RE22,RE25,RE26,RE29,RE30,RE14,RE16,RE18 to 1kohm.	PVT	0.3
66	36	ESD	11/01	ESD request.	1. Reserve J32 and RA86.	PVT	0.3
67		NPI test	11/01	NPI test reserve.	1. Change 0ohm to R-short, RC57,RC40,RC41,RC42,RD3,RD5,RD6,RD12,RD16, RD17,RD22,RD20,RD24,RD30,RD31,RD35,RH149,RH150,RH154,RH8,RH136, RH27,RH87,RH140,RH141,RH86,RH138,RH113,RH135,RH89,R342,R343,R347, R412,RN1~RN3,RN5~RN8,RN10,RN12,RN13,RN16,RN17,R351,RL10,R64~R66, R422,R71,R72,R74,R75,RE52,RE53,RE20,RA1,RA5,RA56,RA79,RA80,RA70~RA72, R353,R355,R358,R374,R375,RV35~RV42,R264,R272~R277.	PVT	0.3
68	30	LAN	11/01	Change LAN solut i ont o E2500	1. Change UL1 to SA0000A6L00.	PVT	0.3
69		EMI test	11/03	EMI test reserve.	1. Change 0ohm to R-short, R96,R97,R383,R384,R109,R110,R121,R122,R111,R112.	PVT	0.3
70	65	Panel	11/03	Add B+ protect fuse.	1. Add F1.	PVT	0.3
71	65	Panel	11/03	Panel design change.	1. Add RG805, depop RG517.	PVT	0.3

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				Custom	C1PR2 LA-E051P
Date: Monday, January 05, 2017				Sheet	102 of 103

Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
72	23	RTC	11/07	Follow PDG.	1. Change RH163 to 1kohm.	PVT	0.3
73	30	LAN	11/23	Change PN.	1. Change LAN IC to R3 PN.	PVT	0.3
74	41,53	GPU	11/23	For AND gate design issue.	1. Change UG22,UG24 to SA00003R000. 2. Change QG502,QG509 to SB000016K00. 3. Change UG22,UG24,RG516,RG558 to +1.8VSDGPU_AON. 4. Change QG502,QG509 gate connect i on GC6_FB_E Nt o 1 8V po w e r a l.	Pre-MP	1.0
75	1	PCB	12/09		1. Change PCB P/N to DAC00006010	Pre-MP	1.0
76	38	EC	12/09	FAN_SPEED connect i on e r r o r	1. correct FAN_SPEED1/ FAN_SPEED3 connect i on	Pre-MP	1.0
77	38	EC	12/09	EC board ID.	1. Change board for pre-MP (R193 to 20k)	Pre-MP	1.0
78	25,28, 45,57	DC/DC	12/14	For load SW design.	1. Add C824~C826, CG922~CG929.	Pre-MP	1.0
79	65	eDP	12/14	For panel design.	1. De-pop Q29,R406. Reverse Q29. Add R808. 2. Change R400 to 2.2k.	Pre-MP	1.0
80	40	BOM	12/16	For NPI debug.	1. De-pop SW2.	Pre-MP	1.0
81	65	eDP	12/16	Panel spec change.	1. Change R405 to 510 ohm.	Pre-MP	1.0

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				Custom	C1PRG LA-E051P	1.0
Date:				Monday, January 09, 2017	Sheet	103 of 103